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Optimization of a High Power-Density Inverter for Automotive Applications by Means of Top-Side Cooled Power Devices

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Abstract

The aim of this paper is to discuss the thermal modeling and simulations performed in the design and the development of a full electro-mechanical leveling system based on wide band-gap power devices operating at high voltage based on top-side cooled transistors. Due to the installation location of the *Electronic Control Unit* (ECU), only air cooling is suitable. For this reason, a good thermal modeling is crucial to allow correct sizing of the whole power stage. The usage of power transistors installed into top-side cooled package eased the task, but the thermal behavior of the whole system has to be verified. The document describes how the thermal models have been done and simulated at two different levels: first, focusing on the chip to evaluate the performance of the package available on the market; second, focusing on the whole ECU for estimating the capabilities of the unit under operating conditions.

1 Introduction

One of the aims of the HiPE [1] EU-funded project is developing a high-voltage fully electro-mechanical leveling system. The final device will be composed of a rotary-to-translation mechanism, coupled with a gear-box to an electric motor, driven by a high-voltage inverter (Fig. 1).

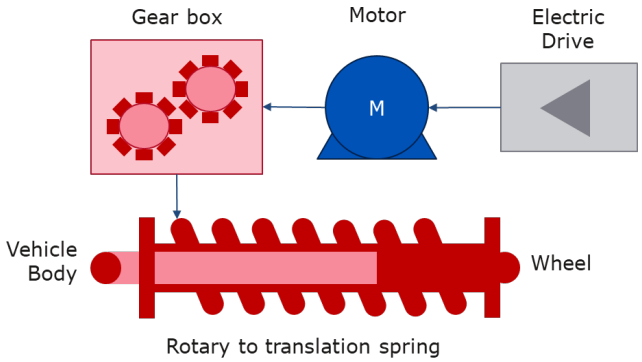


Fig. 1: Schematic structure of the leveling actuator.

The system will be activated by the user every time there will be the need for a different set up given to road conditions. The activation will last few seconds (about 10 s÷20 s) to variate the height of the vehicle from one position to the other. The whole leveling system will be composed of four different actuators, one for each wheel. Each unit will be installed on the suspension. Due to the location of the actuator, liquid cooling of power electronics is not possible, hence it must rely on an effective air-cooling.

In the recent years, some manufacturers have proposed chip packages with a different approach: instead of having the power pad on the bottom, towards the *Printed Circuit Board* (PCB), they started exposing the power pad on the top of the device, to allow a direct contact of the metal part with a heatsink. These chip are called top-side cooled (TSC) devices. Thanks to TSC devices the PCB can be relaxed by the task of heat extraction, easing both its design and fabrication, resulting in a cheaper implementation. From simulation analyses [2] it is possible to reduce the overall thermal resistance by 20%–30%. Since the inverter for the leveling system will be air-cooled, it has been decided to go for *Top-Side Cooled* (TSC) devices in order to reduce the thermal resistance and hence have more margin on the application.

This work summarizes the comparisons of three commercial TSC packages with respect to their thermal performances when used in an ECU in automotive applications. The paper is structured as follows: Sec. 2 describes the thermal investigation of top-side cooled devices, Sec. 3 describes the thermal model of the whole ECU developed so far,

and Sec. 4 draws conclusions providing information and remarks for the final design.

2 Package Comparison

The power devices used in this project are coming from a partner (Nexperia [3]) and for this reason we wanted to evaluate the thermal performance of the package proposed (CCPAK1212i) in comparison of other devices we already evaluated in a different project (AI4CSM, ECSEL JU grant agreement no. 101007326). The approach used here is the same proposed in [2] and will be briefly described in the following paragraphs.

2.1 Methodology

The analysis performed in [2] was focused on understanding the difference between bottom-side and top-side cooled packages, hence a one-to-one comparison between packages in both version has been performed. In this work it is more important to evaluate the effectiveness of the CCPAK1212i package with respect to other ones available on the market from different manufacturers. The packages under investigation are the following:

- TOLT (Infineon);
- PowerPAK® 8x8LR (Vishay);
- CCPAK1212i (Nexperia).

Figure 2 shows these package drawings.
The comparison focused on package performance, mounting the device models on a simplified, but realistic, PCB designed with Siemens' Xpedition Enterprise software [4] and then imported in FloTherm XT [5] for the *Computational-Fluid Dynamic* (CFD) simulation.

2.2 PCB Definition

Joint Electron Device Engineering Council (JEDEC) [6] defines a standard PCB stack-up for thermal resistance characterization that is a 4-layer (2s2p). The Device Under Test (DUT) has then to be measured in still air in a closed chamber [7] This setup is perfect for a fair characterization, independent from any external condition, but is far different from the typical environment where an inverter for automotive applications operates. In those cases, the PCB is dissipated with a heatsink and four layers often are not enough for routing necessity and for reducing the Joule heating. For this reason, we chose a different stack-up: 1.6-mm thick with 6 2-oz layers. This proved to be for us a good trade-off among current capability, thermal effectiveness, and cost. Indeed, it is the stack-up that we use in our inverters. Substrate characteristics have been maintained constant for all the packages to be evaluated (i.e., the same number of layers, copper thickness, and copper percentage).
On the other side, PCB dimensions are package-dependent, since the reason for adopting a new package is to gain some benefit either in thermal resistance or size. For this reason, we planned to make PCB for testing slightly bigger than the actual footprint, to see the benefit of a package in a realistic use case. The drawings with explicit dimensions are shown in Fig. 2 The amount of extra area beyond recommended footprint has been defined to allow the heat to spread to a larger area [8].
Thermal vias are also included and defined to allow good thermal performance, without compromising routing capability and keeping costs reasonable. A good trade-off is a spacing between vias of 1.2 mm [9]. Thermal vias can be realized in different ways and after contacting many PCB manufacturers [10]–[12], we got to these conclusions:

1. Copper-filled vias have the highest thermal conductance, but the process is not so common and thus it is more expensive than traditional solution;
2. Thermally conductive resin provides a negligible improvement since the copper plating dominates the conduction but increases the cost significantly;
3. Filled and capped via (filled with non-conductive resin) provide the best trade-off, allowing via-in-pad for the lowest thermal resistance;
4. Tented vias, where the hole is only covered by solder mask, are the cheapest solution but do not provide any thermal improvement over standard not-filled via.

For these reasons, the PCB for this analysis used only 0.4-mm filled and capped vias.

2.3 Simulation Setup

To setup the simulation environment, PCB definition and mechanical dimensions are not enough. Following assumptions have been made to complete

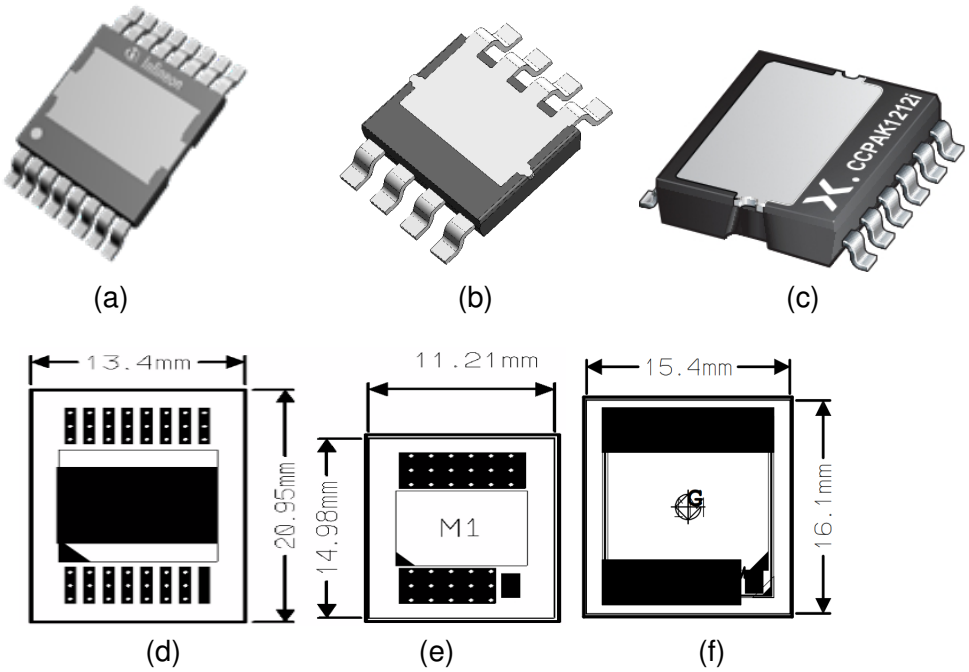


Fig. 2: Package under investigation: TOLT, PowerPAK® 8x8LR, and CCPAK1212i.

the environment and making possible the simulations.

Packages Details about the 3D models have been shared by the manufacturers and include the internal structures of the package.

Materials Each part of the device has been associated with realistic materials with its properties, according to what available from the CFD simulator material library [5], filling what missing with existing literature [13], [14].

Thermal interface material All devices have been put in contact with a *Thermal Interface Material* (TIM) 330 µm thick with a thermal conductivity of 2 W/(m · K)

Environment The target is the automotive environment; hence the environmental temperature has been set to 65 °C using the pressure value at sea level (101 kPa), and a heat transfer coefficient with the air of 10 W/(m^2 · K) [8].

Stimulus Each device has been exposed to the same power to be dissipated. The chosen power was 3 W and 10 W per device, values compatible with continuous and peak usage

To compare the thermal performance of these packages, an equivalent thermal resistance has been defined as the difference between the hot-spot (i.e., the junction) and the surface of the TIM (Fig. 3).

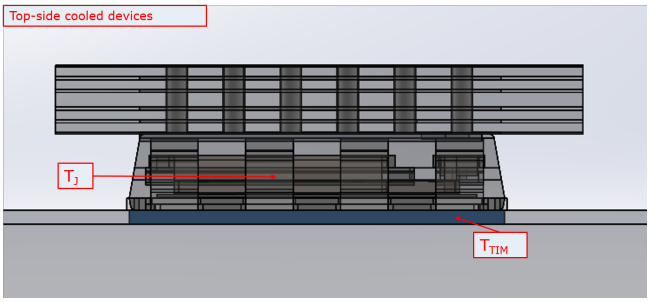
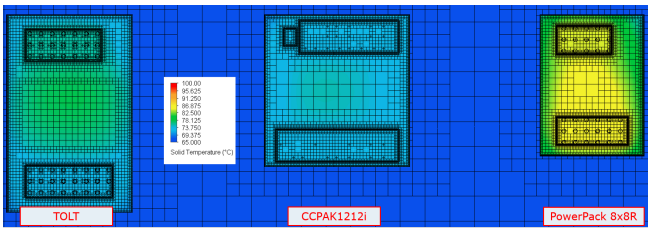


Fig. 3: Measuring point to evaluate the thermal resistance of a package.

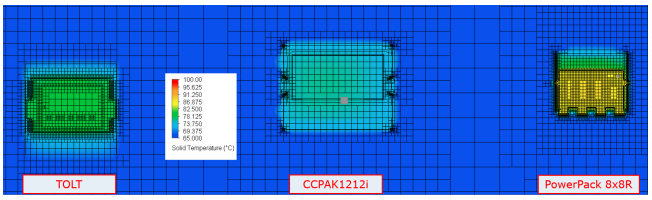
2.4 Results

Simulation results are reported in Figure 4 and Tab. 1 Following some comments on them. The first point to highlight is the correlation of results between the two power levels used. Indeed, thermal resistances for the different packages result independent from the power level. This is an expected result, but it is a way to double-check the correctness of simulation results.

Figure 4 reports the visualization of package thermal distribution by means of a colored scale. The temperature range is between 65 °C (air temperature set) and 125 °C. From this quick visual analysis, it is straightforward to identify the CCPAK1212i as the coolest device. This can be simply explained because the size of the package allows a bigger exchange area towards the heatsink. Indeed, Tab. 1



(a)



(b)

Fig. 4: Graphical visualization of the temperature of the three commercial packages under investigation (a) and of the respective TIM (b).

shows how the the simulated thermal resistance and the exposed pad area are inversely proportional: larger exposed pad area lead to lower thermal resistance. In fact, CCPAK1212i has largest exposed pad area and smallest thermal resistance. To better understand the effectiveness of each package under exam, it is possible to define their *surface power density*, P_D, either referred to the whole device (footprint) or only to the power pad. Hence we can define

$$P_{\mathrm{D,foot}} = \frac{P_{\mathrm{D}}}{A^*_{\mathrm{foot}}}$$

and

$$P_{\mathrm{D,pad}} = \frac{P_{\mathrm{D}}}{A_{\mathrm{pad}}}$$

(A^*_{foot} area has been increased by 1.2 mm on each side to replicate the typical disposition on a PCB, where the devices are close to each other, but not adjacent.) These two metrics have different purposes:

- $P_{D,foot}$ compare the effectiveness of a given solution to produce compact converters, since it express how much power can be handled by the final application; whilst
- $P_{D,pad}$ provides a way to evaluate the technology used to transfer heat out of the chip, since compares the package evacuate heat with respect to the given thermal interface area.

Looking at $P_{D,pad}$ (Tab. 1), the worst case is provided by TOLT package that is based on an old wire-bonded technology, that shows lower thermal capabilities with respect to the PowerPAK® 8x8LR and CCPAK1212i that are both based on copper clips.
Focusing on $P_{D,foot}$, instead the worst case is provided by the PowerPAK® 8x8LR, that shows the difficulties a small footprint to evacuate the heat internally generated. The other two packages are instead more suitable for high power densities, thanks to the wider size of the power pad.
Table 1 shows that CCPAK1212i is the best solution with respect to both metrics. To conclude

- The simulations look consistent, indeed thermal resistances remain constant varying the dissipated power and the dissipation has exhibits physical behavior in the PCB.
- Among TSC packages, thermal dissipation depends (obviously) on the physical dimensions of the exposed pad.
- CCPAK1212i package results the best choice for power applications since provides the lowest thermal resistance with a footprint comparable with other devices.
- CCPAK1212i is the best choice with respect to surface power density.

3 Full ECU Simulation

After having extracted the realistic thermal properties of the packages, these data can be used to setup a full simulation where all the components are present on the PCB to understand the thermal behavior of the whole unit.

3.1 Power Levels

Expected power loss for the devices under test have been calculated using a high-level simulator based on analytical formulae [15]. In this Matlab-based environment it is possible to describe any power transistor only using the parameters available from the datasheet and run simulation on even complex current profiles taking into account also the self-heating of the device. Using this approach, it was possible to generate a curve with the total power losses each device will generate during different operating modes. Figure 5 shows these losses simulated for the transistors under investigation.
To understand the operating point of this application we start from the power characteristics of the target

Tab. 1: Package comparison using surface power density metrics.

Package	Unit	TOLT	8x8LR	CCPAK1212i
TIM k	W/(mK)	2.0	2.0	2.0
TIM thickness	m	300.0E-6	300.0E-6	300.0E-6
Sim Rth	K/W	1.346	1.985	0.879
Tmax	℃	150	150	150
Tamb	℃	70	70	70
Max Power ($\Delta T/R_{th}$)	W	59.4	40.3	91.0
Width	m	10.1E-3	11.8E-3	12.5E-3
Length	m	13.3E-3	8.5E-3	13.5E-3
Area of the package	m^2	134.3E-6	99.6E-6	168.8E-6
Pad Width	m	5.7E-3	6.8E-3	10.8E-3
Pad Length	m	8.8E-3	4.4E-3	5.4E-3
Pad Area	m^s	49.9E-6	29.9E-6	58.5E-6
Surrounding extra width	m	1.2E-3	1.2E-3	1.2E-3
Surrounding extra length	m	1.2E-3	1.2E-3	1.2E-3
Total area (footprint + contour)	m^2	196.3E-6	153.9E-6	236.9E-6
Surf. Power density (Pad)	W/m^2	1.2E+6	1.3E+6	1.6E+6
$P_{D,pad}/P_{D,pad}$(TOLT)	%	100%	113%	131%
Surf. Power density (Package)	W/m^2	302.9E+3	261.9E+3	384.2E+3
$P_{D,foot}/P_{D,foot}$(TOLT)	%	100%	86%	127%

motor, i.e., 2kW. The target output current for 400 V is 6 A. From curves reported in Fig. 5 it is possible to extract the power level for both transistors under case (i.e., 12.7 W). The leveling system is used sporadically for a short duration, and a minimum amount of time must elapse between operations. The expected mission profile is to have a full torque activation for 60 s and then to stop.

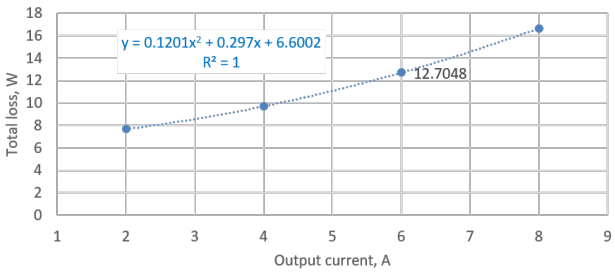


Fig. 5: Power loss estimated for the power transistors used in this application.

3.2 Mechanical Constraints and PCB

The simulation has been done on the existing device, i.e., keeping mechanical dimensions and PCB the same. More specifically, the ECU will be composed of (Figure 6):

- An aluminum base-plate to provide mechanical stiffness and heat-dissipation capabilities to the whole unit.
- A single PCB where both the control unit and the power stage are installed.
- A plastic housing to cover the unit and ensure the sealing against water.

The PCB is defined as

- Standard FR4 dielectric
- 6-layer board, 2-oz copper each

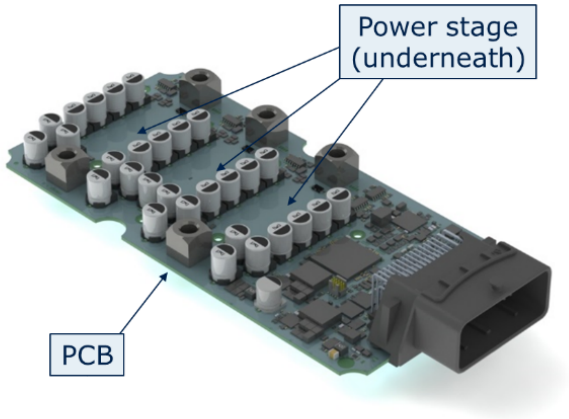


Fig. 6: Rendering of the ECU.

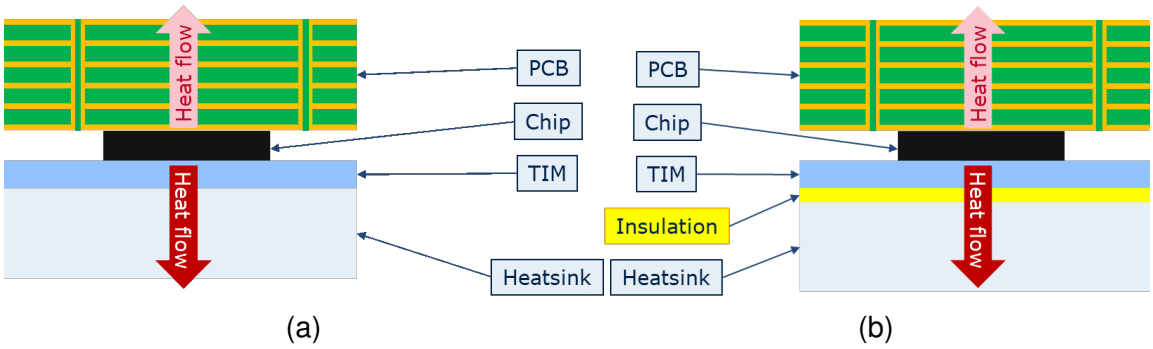


Fig. 7: Material stack-up without any electrical insulation and with electrical insulation.

– Thermal vias filled with resin and capped

The properties of the PCB have been extracted automatically from the electronic CAD [4] by the CFD simulation software used [5].

3.3 Handling High-Voltage

One special mention has to be included related to electrical insulation. Since the application is operating at 400 V, special cares have to be taken into account to segregate this voltage level from being accessible from the outer mechanics and thus avoid any accidental contact. This has been considered during the PCB design, hence both clearance and creepage distances have been kept to make the application intrinsically safe [16]. Unfortunately, the power devices have to be in contact with the aluminum heatsink to dissipate heat, but they have to keep electrical insulation for safety reason. This requires one of the following solutions:

1. Using a TIM that ensures a minimum insulation level between parts (i.e., granting both a minimum thickness and a maximum of conductivity)

2. Using a standard TIM, but inserting an electrical insulation layer between the device and the heatsink to prevent any direct contact.

Both solutions are viable, but adding thermal resistance between the heat source and the heatsink, since high-voltage compatible TIMs have worse thermal properties compared to standard TIMs and adding an insulation layer will generate a similar degradation in the heat extraction capabilities of the ECU (Figure 7).

3.4 Simulation Setup

To setup the simulation environment, PCB definition and mechanical dimensions are not enough. Following assumptions have been made to complete the environment and making possible the simulations.

Packages A simplified two-resistor compact model as specified in [6].

Materials Each part of the device has been associated with realistic materials with its properties, according to what available from the CFD simulator material library [5].

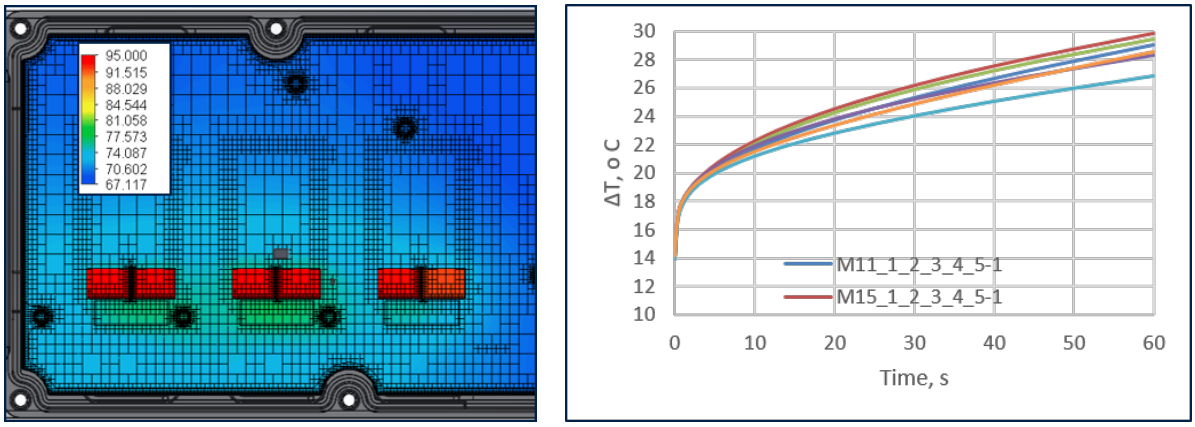
Thermal interface material with a thermal conductivity of 3.5 $W/(m \cdot K)$.

Environment The target is the automotive environment, hence the environmental temperature has been set to 65 °C using the pressure value at sea level (101 kPa), and a heat transfer coefficient with the air of 10 $W/(m^2 \cdot K)$ [8].

Stimulus Each device has been exposed to the same power to be dissipated. According to what expressed in Sec. 3.1.

3.5 Results

The simulation has been performed to verify the thermal behavior of the ECU under expected operating conditions.
Figure 8a is showing the 2-D temperature plot of the ECU exposed to the power loss defined in Sec. 3.1. It is possible to note that the devices on the right are cooler than the others, indeed this is because the right-most part of the board (where the control unit resides) is not modeled, hence the presence of an aluminum base plate at a lower temperature enables a better cooling of the devices close to it. Heat is very localized and provides some valuable information on how much of base-plate can be useful for cooling down the unit properly. Indeed, it would be possible to reduce the heatsink size to the



(a) (b)

Fig. 8: CFD simulation for the transistors used (a) and the transient behavior for their junction temperatures (b).

area to the light-blue area surrounding the power transistors (Fig. 8a) getting a similar cooling effect [17]. This will enable some structure optimization. Indeed, this study suggests it is possible to reshape the unit making it more compact, for instance using a multi-PCB structure.

Figure 8b shows the transient response of the junction temperature of all the MOSFETs in case they are activated and kept operating for 60 s.

The transient curves do not reach the steady state, but the tendency is clear: their behavior is well below the thermal limits, and this enables the ECU to be used even for continuous cycling. This is mostly granted by the TSC adoption, since with bottom-side cooled devices, the thermal resistance would have been 1.5 or 2 times higher making more complex the heat dissipation.

4 Conclusion

The cooling of the leveling system can present an unexpected complexities due to the amount of power required and the almost obliged usage of air cooling. For this reason, this paper has shown how the usage of TSC package can help easing this task and among the package commercially available CCPAK1212i the most efficient.

Thanks to the adoption of this solution, it was possible to optimize the thermal behavior of the inverter driving the leveling system and to make it run cooler, keeping the temperature well below the maximum rating even in case of harsh ambient conditions.

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