High Performance Power Electronics Integrations

Gate driver and power module integration

Part A – Review of Technologies for Power Electronics

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Primary Author	Maurizio Tranchero (I&M)
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Contributors

Name	Organisation	Name	Organisation
Maurizio Tranchero	I&M	Sebastian Klötzer	NEX
Paolo Mercaldi	MAR	Milena Federico	MAR
Annamaria Gianturco	MAR	Gianluca Mastrolillo	MAR
Gaetano Pappalardo	MAR		

Reviewers

Name	Organisation	Date
Bernhard Brandstätter	Virtual Vehicle GmbH	2025-08-22
Kshitij Kolas	Fraunhofer ENAS	2025-08-22

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1. Executive Summary

Power electronics is a foundational technology that is increasingly present across a wide range of applications – from household appliances and high-fidelity audio systems to electric mobility solutions (ranging from e-bikes to hypercars), power grids, and lighting systems. Designing these applications requires a solid understanding of the core concepts and challenges inherent to power electronics.

This document provides a high-level overview of the essential technologies that underpin modern power electronics. It aims to equip readers with the foundational knowledge needed to grasp key challenges and explore potential solutions.

The insights presented in this report are drawn from the combined expertise of three co-authoring companies. Nexperia contributes its deep knowledge as a leading semiconductor manufacturer, while Marelli and Ideas & Motion bring extensive experience in applying power semiconductor technologies to develop innovative power converters for the automotive sector. Although two of the contributors are primarily active in the automotive domain, the principles and technologies discussed are broadly applicable across many industries.

The report focuses on three core areas: power semiconductors, gate driving complexity, and packaging. Each section offers an overview of current solutions, supported by comparative data to facilitate informed evaluation. Every topic concludes with a summary and key takeaways. Additionally, a comprehensive list of references – including academic research and industrial case studies – supports further exploration.

This document also serves as a foundational resource for D4.8 “Report on gate driver integration with power module”, which will delve into the integration of gate driver circuitry and power stages.

Keywords: power electronics, power semiconductors, gate drivers, switching behaviour, packages for power electronics, printed circuit board, insulated-metal substrate, pcb embedding

2. Introduction

2.1 The HiPE Project

The HiPE project is bringing together 13 partners from different European countries, from industrial and research backgrounds covering different segments of the automotive supply chain to develop a new family of high energy-efficient, cost-effective, modular, compact, and integrated power electronics solutions based on wide band-gap technology.

This collaboration aims at achieving the following main objectives of the HiPE project:

- O1: Improve the efficiency of integrated WBG-based power electronics (PE) components and systems by reducing power losses and PE cooling requirements
- O2: Reduce the cost of power electronics components and systems
- O3: Reduce size and weight of power electronics and electric powertrains by enhanced cooling performance
- O4: Increase reliability and dependability through integrated design and intelligent control
- O5: Implement WBG-based power electronics meeting automotive quality levels.

This document summarizes and reviews some relevant power electronics concepts and technologies used in the automotive domain. All the topics are discussed at high level, providing the reader for further readings looking at the external references cited along the document.

2.2 Domain of Application

This document contains concepts mostly related to the power electronics domain, but similar considerations and technologies can be applied to other sector of electronics, e.g., radiofrequency, high-temperature, or space applications. Solutions proposed are typically hard to apply in consumer electronics, due to the high cost they are characterized.

2.3 Objectives

This document tries to summarize technologies used into the power electronics domain, providing the key properties of each solution and comparing it with the alternatives available on the market.

The aim is to produce a basic reference to the technologies behind power conversion application to give a common ground to both power electronics experts and non-experts. This introduction is also used as reference for D4.8, oriented to more advanced technologies.

The document is structured as follows: Chapter 3 introduces the basics of power switches, focusing on different types of transistors and on their building technologies; Chapter 4, instead aims at describing how these transistors must be driven and which are the complexities behind the gate driving. Chapter 5 discusses about packaging technologies, i.e., the way power devices are connected and interacting with the physical world.

2.4 Acknowledgments

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3. Power Transistor and Technology

3.1 Transistors

This section introduces the transistors typically used in power application. Describing all these device families in detail is beyond the scope of this report. The main aim of this document is to summarize the advantages and drawbacks of these transistors when used in the power conversion domain. The reader is encouraged to deepen their knowledge more on this topic. Good starting points are [1] and [2].

3.1.1 BJT – Bipolar-Junction Transistors

Bipolar Junction Transistors are the first transistors which appeared on the marked and are formed by putting two PN junctions aside. The name of the BJT already hints at some key characteristics that also lead to drawbacks, which are common in other transistor families (i.e. IGBT, described later):

- It is a *bipolar* device; therefore, conduction current is carried by both holes and electrons, i.e., minority and majority carriers, and this results in some drawbacks when trying to switch them on and off fast. Recombination time for carriers is reversely proportional to their concentration levels; hence minority carriers are not recombining at the same rate and are much slower compared to majority ones. This is particularly evident when a device is switched off, since the time required to empty its spatial charge region is longer, causing extra losses.
- The current passes through a *junction*, hence there is an immediate contribute on power losses due to the built-in voltage of the junction. This is provided by the type of material used in the junction; therefore, the power losses cannot be reduced unless the semiconductor pairs used are changed. Comparing a junction device with an ohmic one, it can be seen that conduction losses will behave as depicted in Table 3-1: At low currents FETs are more efficient, but for higher currents the effect of the junction will have less impact, compared to the effects given by resistive losses.

Another disadvantage of BJT is related to its intrinsic structure. To withstand high breakdown voltage, the base has to be thick, but a thick base means low trans-conductance, i.e., low ratio between control current (base current) and output current (collector current). A typical value is around 10 for 500 V blocking voltage (see Table 3-1). This means that, to use a BJT for high-voltage applications, a continuous base current – typically only ten times smaller than the desired output current – must be provided. This makes the usage of BJT unsuitable for high voltage applications (i.e., above 1 kV).

Table 3-1: Comparison between commercial BJTs.

Device	Producer	$I_{CE,max}$ [A]	$V_{CE,max}$ [V]	$V_{CE,sat}$ [V]	$h_{FE,min}$
STL73	STM	1.5	700	1.0	4
BFN18	Infineon	0.5	300	0.5	25
MJL4281A	On Semi.	15	350	1.0	10

3.1.2 MOSFET – Metal-Oxide-Semiconductor Field-Effect Transistors

Metal-Oxide-Semiconductor Field-Effect Transistor is a family of devices basing current conduction on majority carriers. Putting a given amount of charge on the control pin (*gate*) recalls opposite charges on the other side of the insulator, as it happens in a capacitor. This amount of majority carriers modulates the resistance (channel) between other two terminals (*drain* and *source*).

MOSFETs have some key differences compared to BJTs:

- Static control current is zero, i.e., the gate behaves like a capacitor terminal, hence we can control high output currents with theoretically zero control current. (Actually, the current is not zero during transitions from off to on and vice versa.)
- They are the majority devices, therefore there are not any effects related to the extraction of minority carriers (i.e., tail current). The resulting device is much faster during commutation, compared to equivalent bipolar ones.
- Losses are mainly due to the resistive intrinsic zone. This leads to losses proportional to the square of the current passing through the device.

The latter characteristic makes MOSFETs unsuitable for high current usage, since losses are increasing according to a quadratic law, making heat extraction more and more difficult when current increase.

3.1.3 IGBT – Insulated-Gate Bipolar Transistor

The *Insulated-Gate Bipolar Transistor* is another family of devices crucial for power application. They can be seen as the combination of a MOSFET (input) and a BJT (output), resulting in perfect trade-off between the two families. IGBTs are suitable for high current application because:

- FET input allows to decouple control current from output one, making possible the drive of high output currents without needing a high continuous control current.
- BJT output allows quasi-linear losses with respect to the current passing through the device, making a great advantage compared to MOSFETs (see Figure 3-1).

IGBTs are suitable for high voltage application because their contribution to total losses increases linearly (or slightly more than linearly), whilst for MOSFETs the increase is quadratic with current.

The ensemble of characteristics of IGBTs make this family suitable for high power applications (see Figure 3-1).

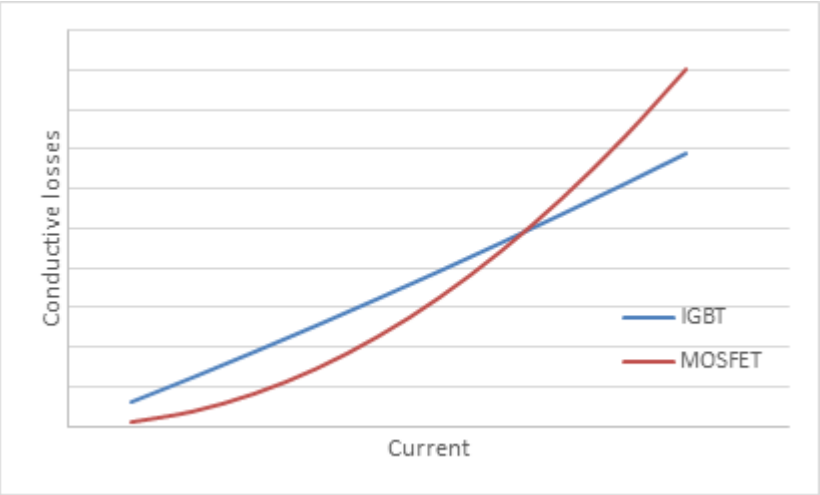

Figure 3-1: Comparisons of IGBTs and MOSFETs conduction losses with respect to current.

3.1.4 HEMT – High Electro-Mobility Transistor

The *High Electro-Mobility Transistor* is a field-effect device based on materials with different bandgaps (hence the name hetero-junction). The junction is formed at the interfaces between the materials involved: the difference of donors' concentration between the two materials generates a two-dimensional “gas” of electrons (2DEG) that can be modulated by applying a voltage between the two materials. This two-dimensional surface is the channel of the device.

The 2DEG is not composed of a doped channel as it happens in the case of the MOSFET, hence the number of ionized donors is smaller, reducing significantly scattering, resulting in a structure characterized by high electro-mobility [3]. This advantage is obtained by higher complexity of the structure, hence the corresponding cost results higher [4].

Typical hetero junctions are composed of AlGaN/GaN, AlGaAs/GaAs, InGaAs/GaAs, and Si/SiGe. The devices available on the market are based on AlGaN/GaN and AlGaAs/GaAs. They are also known as heterojunction field-effect transistors (HFET)

GaN devices have a lateral structure as shown in Figure 3-2. Everything starts from a substrate that can be made of pure silicon, silicon carbide, or silicon on insulator. To adapt different lattice structures of the chosen substrate and GaN, a transition layer is inserted. The actual device starts from here with an intrinsic GaN layer, usually grown through chemical vapour deposition process.

On the surface of this layer, a thin AlGaN layer is grown. The properties of this material produce a two-dimensional electron gas at the interface. This makes the contact between source and drain connected even when the gate is not biased (a normally on device). Thanks to this structure the resulting resistance between source and drain is very small.

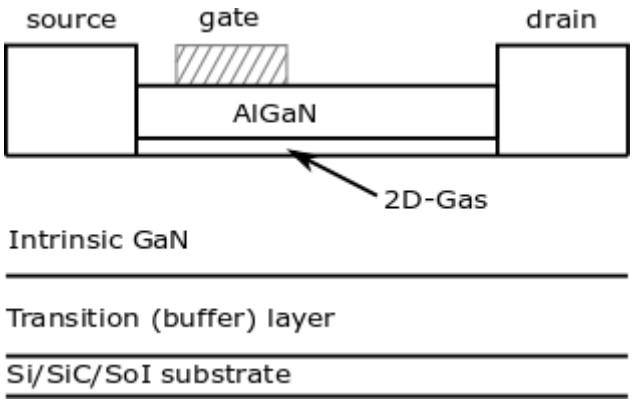

Figure 3-2: Structure of a GaN HEMT.

These transistors are depletion-mode devices, that is, devices that are normally on, without the need for applying a gate bias. A negative gate bias is then needed to switch the transistors off. This biasing is not straightforward and is considered inconvenient by most of power conversion application, where it is impossible to guarantee the avoidance of any shoot through between power rails at power up. (HEMT are still in use and guarantee the highest performance in switching speed.)

GaN products are termed High-Electron Mobility Transistors (HEMT), a name that captures one of the intrinsic benefits of GaN: the high electron drift velocity. This HEMT structure is based on the unusually high electron mobility, described as a two-dimensional electron gas (2DEG), near the interface between an AlGaN and GaN hetero structure interface. 2DEG is a gas of electrons free to move in two dimensions but tightly confined in the third. So, these GaN transistors need no doping because the current relies on 2DEG. The first gallium nitride metal semiconductor field-effect transistors were experimentally demonstrated in 1993. They are still considered the only major GaN transistor family and are still being actively developed.

The first GaN HEMT was called d-mode HFET (depletion mode, H for high power) due to the fact that a negative voltage relative to both drain and source electrodes was needed to turn the device off. These transistors are depletion-mode devices, that is, devices that are normally on, without the need for applying a gate bias. A negative gate bias is then needed to switch the transistors off. This biasing is not straightforward, and it is not easy to handle in power conversion. Today there’s the opportunity to use depletion mode, normally-on devices in a majority of power electronic circuits (using DC enable switch-based topologies), several topologies such as AC/AC converters used for motor drive actually are superior when implemented with the inherently bi-directional capable depletion mode GaN based HEMT devices [5, 6].

A Cross section of this structure is shown in Figure 3-2. Notice the additional layers of metal are added to route the electrons to gate, drain, and source terminals. This structure is repeated many times to form a power device. A positive bias on the gate relative to the source causes a field effect which attracts electrons that complete a bidirectional channel between the drain and the source. Since the electrons are pooled, as opposed to being loosely trapped in a lattice, the resistance of this channel is quite low. When the bias is removed from the gate, the electrons under it are dispersed into the GaN, recreating the depletion region, and once again, giving it the capability to block voltage. With zero bias gate to source, there is an absence of electrons under the gate region. As the drain voltage is decreased, a positive bias on the gate is created relative to the drift region, injecting electrons under the gate. Once the gate threshold

is reached, there will be sufficient electrons under the gate to form a conductive channel. The benefit to this mechanism is that there are no minority carriers involved in conduction, and therefore no reverse recovery losses. While Q_{RR} is zero, output capacitance (C_{OSS}) has to be charged and discharged with every switching cycle. For devices of similar $R_{DS(on)}$, GaN transistors have significantly lower C_{OSS} than silicon MOSFETs. As it takes threshold voltage to turn on the GaN transistor in the reverse direction, the forward voltage of the “diode” is higher than silicon transistors [7].

One can compare this devices behaviour to that of Si MOSFETs. They both behave similarly but with some differences:

- $R_{DS(on)}$ versus VGS curves are similar to MOSFETs
- The temperature coefficient of $R_{DS(on)}$ of the eGaN FET is also similar to the silicon MOSFET as it is positive, but the magnitude is slightly less
- The threshold of Gallium Nitride transistors is lower than that of silicon MOSFETs
- Starts to conduct current at 1.6 V
- This is made possible by the almost flat relationship between threshold and temperature along with the very low C_{GD}, as described later
- The lateral structure of the GaN transistor makes it a low charge device, resulting in an extremely low C_{GD} (Capacitance) which leads to the very rapid voltage switching capability of GaN transistors (MHz region), a unique characteristic compared to silicon and SiC devices
- Horizontal structure makes it hard to manage a relatively high current, although this can be effectively addressed through the use of front side solderable devices and dual sided surface mount packaging techniques, which is still being developed [8]
- Low C_{GS} (compared with silicon MOSFETs) giving them very short delay times, and good controllability in low duty cycle applications
- No minority carriers involved in conduction, and therefore no reverse recovery losses
- The low gate resistance also helps the dV/dt immunity.

3.2 Semiconductor Technology

The power semiconductor landscape has evolved dramatically, catering to the expanding demand for more efficient, compact, and powerful electronic devices. This section delves into the fundamental aspects of power transistor technology, examining structural innovations and material advancements that shape modern power electronics. For further readings, it is possible to refer to these references [9, 10].

3.2.1 Lateral vs. Vertical

Power transistors can be broadly categorised based on their structural design: lateral and vertical (Figure 3-3). *Lateral* power transistors, such as GaN-based High Electron Mobility Transistors (HEMTs), leverage a two-dimensional electron gas (2DEG) channel formed at the interface of hetero structures. These devices are generally grown on non-native substrates such as silicon to reduce costs and are characterized by their high-frequency performance due to reduced gate charge and on-resistance. The lateral design is dominant in applications requiring compact and light-weight systems, such as consumer electronics and RF amplifiers [11].

On the other hand, *vertical* power transistors- standard in silicon and emerging in SiC and GaN- are designed to handle higher currents and voltages. The current flows perpendicularly from the top to the bottom of the device. This configuration allows better heat dissipation and less resistance for current conduction at high power levels. As a result, vertical transistors are preferred in high-power applications such as electric vehicle inverters and industrial motors, where robustness and thermal handling are paramount. The advent of vertical GaN devices is anticipated to further these capabilities, offering potential reductions in device size and cost while maintaining high efficiency.

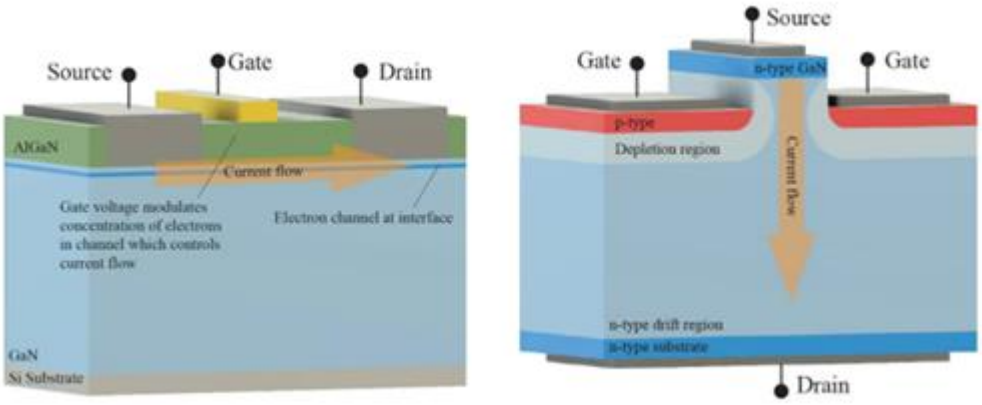

Figure 3-3: Lateral (left) and vertical (right) GaN devices [12]

3.2.2 Planar and Trench Technology

Planar and trench technologies represent two critical developments in semiconductor manufacturing (Figure 3-4). Planar transistors, known for their simpler manufacturing process, have historically been the mainstay of semiconductor devices. They feature a horizontal channel and are easier to fabricate, making them cost-effective for many applications. However, the performance and scaling limitations of planar designs, especially in reducing on-resistance for high-voltage applications, have directed the industry towards trench technologies.

Trench technology addresses many of the limitations of planar designs by embedding the gate electrodes in vertical trenches carved into the substrate. This design enhances the gate control over the channel, allowing higher current density and faster switching speeds. It reduces the device's footprint, enhances thermal efficiency, and provides finer control over the electric field, crucial for reducing power losses. The super-junction MOSFETs employ trench technology to significantly reduce on-state resistance, extending the operational voltage range beyond what is achievable with planar technology.

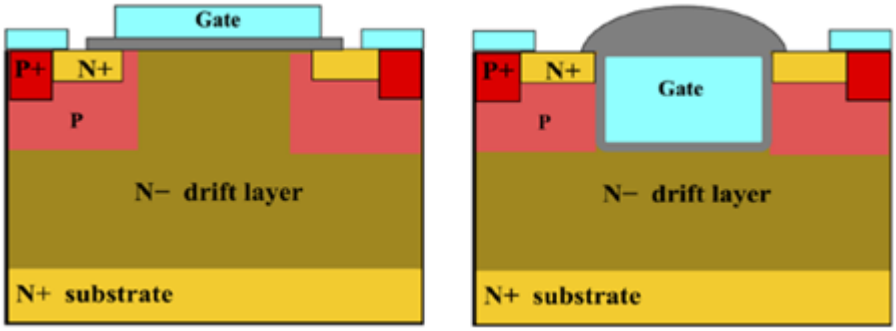

Figure 3-4: SiC MOSFET planar (left) and trench (right) [13]

3.2.3 Silicon vs. Wide Band-Gap Devices

The exploration of power devices has shifted focus from traditional silicon (Si) to Wide Bandgap (WBG) materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) due to their superior electronic properties. Silicon has been the cornerstone of semiconductor technology since the 1970s. However, the growing demand for higher efficiency and power density in electronics, especially within automotive applications, has unveiled the limits of Si-based devices. The WBG materials offer enhancements over Si, notably in terms of energy efficiency and thermal performance, addressing the crucial needs of modern power applications.

The emergence of wide bandgap (WBG) semiconductor materials presents a transformative shift in power conversion technology. Where traditional silicon (Si) devices once dominated, materials like Silicon Carbide (SiC) and Gallium Nitride (GaN) now offer superior electronic properties that contribute to increased efficiency, reduced losses, and broader application potential. These WBG materials are characterized by their ability to operate at higher voltages, temperatures, and frequencies than Si, allowing a wide array of applications in modern power electronics, especially in the automotive and specialized fields like motorsport.

Table 3-2: Comparison of WBG material with S [13].

Properties	Si	6H-SiC	4H-Sic	GaN
Thermal conductivity, W/(m K)	150	490	490	130
Band gap, eV	1.12	3.03	3.26	3.45
Breakdown field, kV/mm	30	250	220	330
Dielectric constant	11.9	9.66	9.7	8.5-10.4
Electron mobility, $cm^2/(Vs)$	1500	400	800	2000
Drift velocity, 10^5 m/s	1.02	2	2	2.2
Intrinsic carrier concentration, cm^{-3}	10^{-1}	10^{-9}	10^{-6}	10^{-10}

3.2.3.1 SiC - Silicon Carbide

Silicon Carbide (SiC) is one of the most used WBG materials and has become a pivotal component in the landscape of power electronics. The intrinsic properties of SiC, such as its high thermal conductivity and critical electric field strength (Table 3-2), make it suitable for high-power and high-temperature applications. Since SiC can operate at temperatures up to

200°C with minimal thermal management requirements, it becomes an optimal choice for automotive inverters where weight and size are critical.

The transition to SiC devices enhances efficiency by reducing on-state resistance (RDS(on)) and offering faster switching times, thereby minimizing power losses. SiC technology has penetrated the electric vehicle market, focusing on applications like traction inverters and DC/DC converters. While the initial cost of SiC devices can be higher than their Si counterparts, the long-term benefits, including reduced system size and improved efficiency, are driving rapid adoption in sectors prioritizing sustainability and performance.

Silicon Carbide (SiC) is renowned for its excellent thermal stability and high voltage handling capabilities, making it ideal for high-temperature and high-power applications. Its ability to conduct heat more efficiently than silicon, due to a thermal conductivity approximately three times greater, significantly reduces thermal management challenges in power modules. This property is especially beneficial in high-demand environment where power modules operate under extreme thermal conditions.

SiC's wide bandgap allows for higher breakdown voltages and lower conduction losses, thus enabling the design of more compact and efficient power electronics. The inherent physical robustness of SiC devices supports their deployment in applications requiring superior reliability and longevity, such as electric vehicles and high-performance automotive applications. Despite its cost compared to Si, the performance benefits and reliability of SiC justify its growing adoption in power modules used in highly demanding applications.

3.2.3.2 GaN - Gallium Nitride

Gallium Nitride (GaN), another wide band-gap semiconductor, is rapidly gaining attention for its high electron mobility and breakdown voltage capabilities. GaN devices surpass Si, and in certain contexts, SiC, in high-frequency applications thanks to lower gate charge and faster switching capabilities (Table 3-2). This translates to significant size and weight reductions in power conversion systems, which is a significant advantage for electric vehicles and data centres.

Initially adopted in radio frequency (RF) applications, GaN technology is now expanding into consumer electronics, telecommunications, and increasingly into automotive sectors. As a lateral structure semiconductor, GaN devices utilize hetero structures grown typically on non-native substrates like Silicon (Si), enabling cost-effective production. However, one of the ongoing challenges for GaN devices is managing thermal dissipation in high-power applications, which SiC handles more adeptly due to its superior thermal properties.

In the broader field of power semiconductors, GaN and SiC are seen as complementary technologies, each with unique advantages. SiC’s robustness and thermal properties suit high voltage, lower frequency operations, whereas GaN’s efficiency at high frequencies opens new potentials for tightly integrated power systems. As the industry continues progressing towards higher sustainability and efficiency standards, GaN and SiC are jointly redefining power electronics, setting new benchmarks for performance and reliability.

Gallium Nitride (GaN) offers compelling advantages for high-frequency and high-efficiency applications. Its high electron mobility and saturation velocity allow GaN devices to perform exceptionally well in fast-switching environments, making them ideal for RF applications and power conversion systems where size and weight reductions are critical. GaN's lateral

structure facilitates integration on silicon substrates, lowering production costs and allowing the use of existing semiconductor manufacturing infrastructures.

GaN transistors typically adopt high electron-mobility transistors (HEMT) configurations, which are lateral devices that can achieve very low on-resistance and enable fast switching. However, the downside of this lateral design is its unsuitability for very high-power applications because of thermal management and current handling limitations compared to vertical structures like those in SiC technologies. Nevertheless, ongoing research and advancements are attempting to develop vertical GaN structures to expand GaN's applicability in high-power domains.

The deployment of GaN necessitates careful consideration of circuit design to mitigate potential drawbacks like thermal stress and substrate compatibility, particularly when dealing with high power densities and fast switching activities. Nonetheless, the combination of reduced conduction losses and increased operating frequencies presents GaN as a strong candidate for specific high-performance segments, offering opportunities to innovate power module designs optimally suited for compact and efficient power electronics systems.

3.3 Comparison

Understanding which is the best solution for a given power application is not always straightforward. The typical graph used to determine when to apply the transistor technologies described above is shown in Figure 3-5.

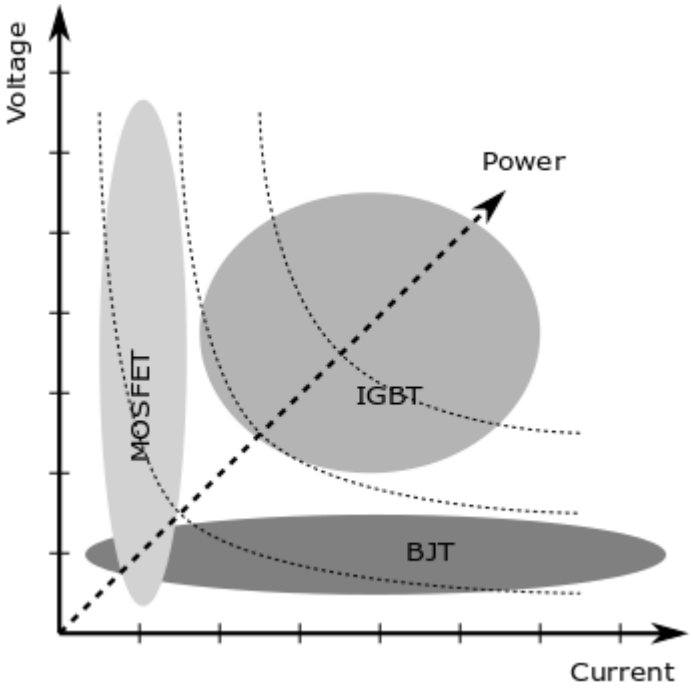

Figure 3-5: Field of application of different transistor technologies.

BJTs were used in a small niche of application, low voltage and medium-high current. Due to the technology advancements that brought drain-source resistance to very small values, nowadays, it is more common to have silicon MOSFETs covering also this part of the graph.

MOSFETs are well suited for low current applications, i.e., where the average current is below the maximum current the device can withstand. This due to the intrinsic characteristic of the

device, since its losses are proportional to the square of the drain current, it is more efficient to use these devices for low currents (Figure 3-1).

IGBTs are characterized by their current capabilities, and this is very visible in industrial field, were the vast majority of applications is done with IGBT. Indeed, where cost is crucial and the dimension of the final controller (included EMI filter and cooling) is not an issue (industrial cabinets can host comfortably big units), the best choice is to go for IGBTs.

HEMT, instead, are characterized by high electro-mobility, hence they are very suitable for high-speed applications. (In radiofrequency applications gallium-based heterojunctions are leading.) Silicon based HEMT have been produced for research but are not present on the market. This is mainly due to the higher complexity and hence higher cost related to the manufacturing process. In fact, a costlier process must be justified by the performances brought by the device. And GaN (or GaAs) devices are outperforming Si-based hetero structures. On top of this, the fact that this structure is intrinsically lateral plays a significant role. Indeed, having all the terminals on the same side of die reduces stray parameters, enhancing high-frequency commutation capabilities. But this comes not for free: a lateral structure is less suited to handle high voltage. This is the main reason why GaN transistors are mostly available up to 650 V. With respect to current capabilities are still behind the current density for SiC MOSFETs [14]. The low stray inductance and the high electro-mobility are making this component suitable for DC-DC power converter, were the request reducing the room for magnetic components is pushing the switching frequency close to the MHz level.

3.3.1 Thermal Behaviour

Looking at thermal behaviours, different technologies behave also differently. Figure 3-6 plots the normalized temperature variation for drain-to-source on-resistance for several commercial power modules and transistors based on different materials. From the graph it is possible to extract several important notes:

- Silicon is a mature technology and hence its variations with temperatures are consistent among different devices and manufacturers (the three green lines are almost superimposed).
- SiC has a higher stability with temperature than silicon, but due to the relative novelty of the material and the advances each technological step provides, it is possible to have significant variation changing device or manufacturer (blue lines are all below green ones).
- GaN shows even a higher variability spread because of its less mature process: each technological step provides huge improvement in process stability (yellow lines).

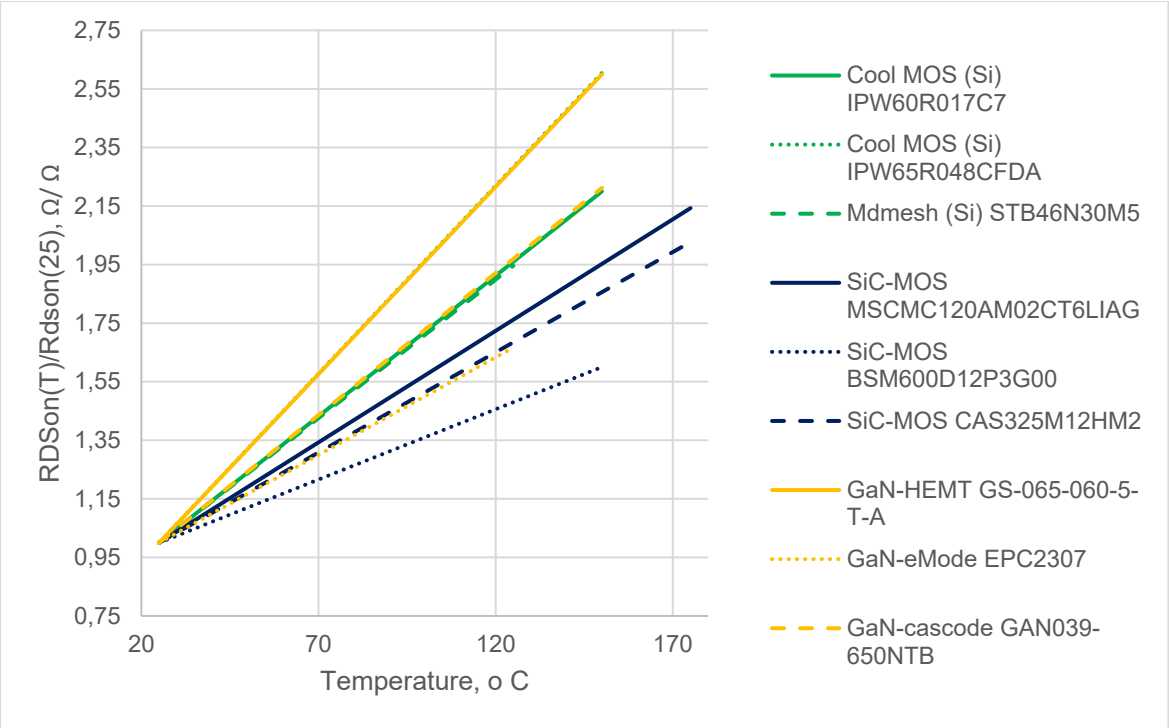

Figure 3-6: Normalized $R_{DS(on)}$ variations vs. temperature for different commercial power transistors.:

3.3.2 Considerations

SiC is one of the most appealing technologies at present for power inverter. Indeed, its low switching losses, high breakdown voltage withstand capability, and high current density polarized the discussion in both academia and industry fields. What it is not always discussed is the impact of costs. Indeed, these devices can achieve higher efficiency with respect to the IGBT counterparts because they can reduce both switching and conduction losses (especially in the average case), but the cost can be between twice and three times higher for a target current. Recently, some manufacturers announced to start the production of 200-mm SiC wafers [15], while only few are still with 150-mm size wafer, but the manufacturing yield is lower compared to silicon one [16]. Slicing an SiC ingot is still more complex and a low-yield process (the material is very hard and brittle, forcing to make thicker wafers and to waste about the same quantity of material during slicing). Moreover, the hardness of the substrate requires to use expensive tools that are more subject to wear out than those for Si wafers. This is why cost will probably not decrease dramatically in the next years [17].

So far, the focus has mainly been the inverter. But this is not the only actor playing a role. In a e-powertrain there are other two important players: the battery and the motor. It is important to remind that the total efficiency is the product of the efficiencies of the three units: to get an actual efficiency improvement it is important to increase it overall and not simply shifting losses from one unit to the others. For instance, reducing the switching frequency of the inverter can improve the inverter efficiency, since switching losses are proportional to frequency. But at the same time this increases losses on the motor (high order harmonics are converted either in vibration or heat and hence wasting energy) potentially increasing the load on the cooling system. On the other side, reducing the harmonic content on the motor helps reducing the heat to be extracted from it, but forces the inverter to switch faster (or to use multi-level topologies) in order to reduce the spurious frequencies that are not converted into torque. This kind of system-level optimization is rarely performed, since many companies are producing a single

device in the powertrain and hence, they cannot do this level of optimization. Companies integrating the final application are often looking at optimizing the price for the separate components. But system-level simulation is key to make well-sized, efficient systems, able to exploit as much as possible the capabilities of the single components.

Since cost drives most of the productions, it is foreseeable that for high-end, high-profit, high-efficient, harsh environment applications (i.e., top-class automotive, aerospace, or defence), SiC will be the preferred choice. On the other hand, for low-end, low-profit, standard applications (i.e., home appliance, economy cars, industrial) the preferred solution will be to use IGBTs and Si-MOSFETs, when possible. These scenarios definitely provide some room for GaN devices, due to their lower cost compared to SiC and higher performances respect to silicon.

4. Gate Drivers

The gate driver plays a pivotal role in a power converter, independent of the technology and semiconductor material used for the switching transistors. The gate driver must be matched precisely with the transistor that is being driven, and it must perform reliably across a wide range of temperatures, voltage and current levels as well as normal and abnormal operating conditions during the entire operating life. To achieve best switching performance and efficiency as well as high reliability, robustness and good electromagnetic compatibility (EMC), modern power semiconductors are the key components, but they can only shine if the gate driver is up for the task as well. In this chapter, an overview on the requirements and features of modern gate drivers for use with state-of-the-art wide bandgap semiconductors is given, with focus on use in half-bridge based circuits.

4.1 Switching Behaviour

First, it is necessary to describe briefly switching behaviour of current and voltage in a SiC power MOSFET. (The discussion can be adapted to IGBT too, by simply changing drain with collector and source with emitter.)

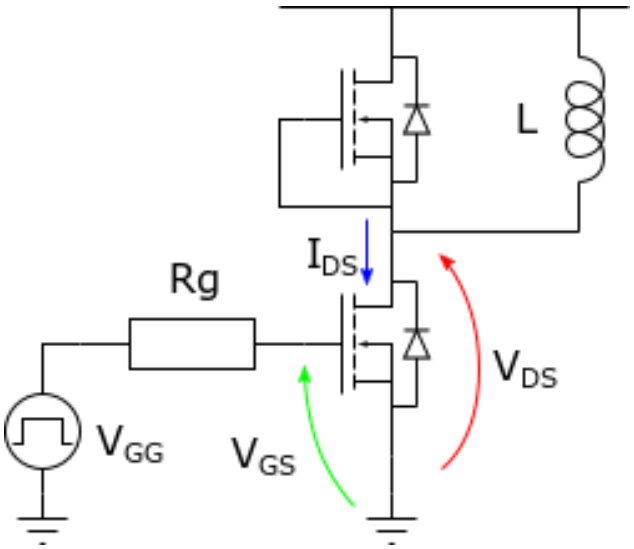

Figure 4-1: Half-bridge configuration used for switching description.

The half-bridge structure shown in Figure 4-1 is used to describe switching waveforms drafted in Figure 4-2 that are representing the expected behaviour of gate-to-source voltage, drain-to-source voltage, and the drain current. (Pictures are not to scale.)

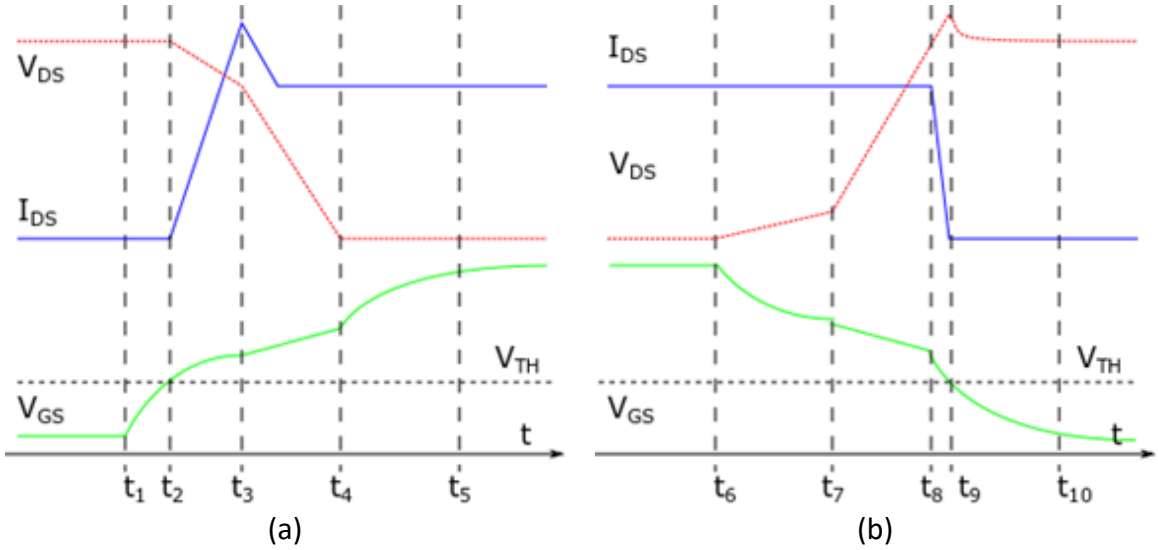

Figure 4-2: Simplified waveforms of V_{GS}, V_{DS}, and I_{DS} in a SiC MOSFET during switch on (a) and switch off (b).

During *switch-on* commutation (Figure 9-a) output waveforms, V_{DS} and I_{DS}, change according to the voltage seen between gate and source pins (V_{GS}), hence:

- Until V_{GS} is below on threshold (V_{TH}), I_{DS} and V_{DS} are stable.
- Above V_{TH} (t_2), output current starts ramping up until it reaches its maximum value, given by the sum of load and reverse-recovery currents of opposite switch diode (t_3). During this period, V_{DS} reduces due to output current variation on stray inductance.
- At this point the MOSFET enters the Miller region (t_3-t_4), where its gate-to-drain capacitance changes according to output variation. In silicon MOSFETs V_{GS} maintain this value until output voltage has completed its transition, whilst in SiC devices this value increases linearly due to the high non-linearity of C_{GD}.
- In the last part of the transition (t_4-t_5), the MOSFET settle to a stable resistive value, depending on the steady-state gate voltage level.

During switch-off commutation (Figure 9-b) output waveforms change in the opposite order:

- In the first phase (t_6-t_7), the MOSFET moves in the ohmic region because of the gate voltage decrease.
- In t_7 it enters Miller zone and output voltage start increasing up to the DC bus level, reached in t_8.
- In t_8 output current commutation starts and this causes a voltage drop on stray inductance that sums up to the DC bus level and produces a voltage overshoot at MOSFET drain-source terminals.
- Current stops flowing when V_{GS} reaches V_{TH} (t_9) and the MOSFET goes off.

From switching waveforms, we can draw following considerations:

- Switching losses are proportional to switching time, indeed, the longer drain-source voltage and currents stay overlapped, the more power is wasted.
- Fast switching is related to high voltage and current variation over time, hence reducing switching time by means of steeper voltage and current transitions will result into higher stresses (i.e., higher voltage overshoots) and higher electromagnetic noise.

These two considerations above are apparently opposite, since on one side we would like to reduce switching time to improve efficiency, but on the other we need to get rid of EMC issues and devices overstress. It is clear that there are some phases of the switching process where we can work to accomplish the first consideration without affecting the second one. On the other side, we can reduce steepness of current and voltage transitions, without affecting the overall switching time.

Looking more carefully at simplified waveforms in Figure 9 we can identify following operating regions:

- *Off phase* (before t_1 and after t_{10}), where the power device withstands the DC bus voltage and does not allow any current flowing.
- *Sub-threshold phase*, where the device starts (or completes) its transition ($t_1<t<t_2$ and $t_9<t<t_{10}$); timings depend on gate capacitance, gate resistor, and gate voltage applied.
- *Current commutation phase*, where output voltage is substantially fixed while current changes ($t_2<t<t_3$ and $t_8<t<t_9$); also, in this case timings depend on gate capacitance, gate resistor, and gate voltage applied.
- *Voltage commutation phase*, also known as *Miller region*, where output voltage swings from one state to the other; this region is where Miller effect take place ($t_3<t<t_4$ and $t_7<t<t_8$); timings depend on current capabilities of the driver and total gate charge required to pass the Miller region.
- *Ohmic phase*, where voltage has been commuted, the transistor is fully on, but resistive value of the channel depends on V_{GS} ($t_4<t<t_5$ and $t_6<t<t_7$); timings depend on gate capacitance, gate resistor, and gate voltage applied.
- *On phase*, where the device completed its transition and waits for next command ($t_5<t<t_6$).

It is easy to see that changing either gate voltage, gate current, or gate resistor during commutation can affect timings of one or more phases above.

Previous considerations lead to Table 4-1. From this table, multiple optimization strategies can be viable, e.g.:

- Focusing on sub-threshold phase, it is possible to see that reducing the amount of time to reach V_{TH} decrease switching time overall, but this will not affect switching losses.
- Voltage and current commutation phases can be shortened to reduce time where voltage and current overlap, hence improving switching losses, but this will directly result into higher d*v*/d*t* and d*i*/d*t* and thus will produce more EMC issues and will stress more motor windings.
- Increasing the duration of voltage and current commutation phases would decrease EMC and stress, at the expense of commutation losses.
- Voltage slopes are directly linked to conducted disturbances and winding insulation degradation. A possible optimization strategy to increase winding's life is to reduce d*v*/d*t* when switching losses are smaller (i.e., when load current is lower), while increasing them when switching losses are becoming unsustainable.
- It would be possible to adapt current variation slope to keep it constant, regardless the load current, hence optimizing for ringing and radiated disturbances levels by changing the driver's strength inversely proportional to current level.

- Subtler strategies could aim at reducing the current switching speed at the end of current commutation phase, just before t_3, to decrease the current overshoot (and eventually oscillations) due to body diode Qrr of the complementary MOSFET.
- Similarly, reducing the current switching speed at turn off (t_8 to t_9) will decrease the voltage overshoot due to voltage drop on parasitic inductance.

There are multiple ways to reduce these timings, voltage applied (V_{GG}) can be dynamically changed, the same can apply for gate resistance (R_G), or even to use current drive with variable strength.

Table 4-1: Effects of "relaxed" and "nervous" transition on each switching phase.

	Transition	
Region	**Relaxed**	**Nervous**
Off	N/A	N/A
Sub-threshold	Increases switching time	Reduces switching time
Current commutation	Reduces ringing Reduces radiated EMI Reduces voltage overshoots Increases switching losses	Increases ringing Increases radiated EMI Increases voltage overshoots Reduces switching losses
Voltage commutation	Reduces common-mode noise Reduces stresses on motor windings Increases switching losses	Increases common-mode noise Increases stresses on motor windings Reduces switching losses
Ohmic	Increases switching time	Reduces switching time
On	N/A	N/A

4.2 Basic Requirements and Advanced Gate Drive Features

The basic functionality of a gate driver and the different phases of the turn-on and turn-off switching transitions have already been briefly described in section 4.1 using the example of a SiC MOSFET. The explanations given are largely independent of device technology and can be applied to most normally off power transistors. However, there are significant differences in the operating parameters of the various types of wide bandgap devices available on the market today. Table 4-2 gives an overview over various parameters that are relevant for designing the gate driver in comparison to a Si IGBT.

To achieve good performance, the complete gate drive circuit, including its signal chain, power supply circuitry and integrated circuit for driving the gate must be selected carefully to match the requirements of the power transistors. Figure 4-3 gives an overview of some of the key elements that must be considered when designing a gate drive circuit and lists some of the special features offer by modern gate drivers that help to enhance performance, safety and reliability.

Table 4-2: Overview of most common values for various device technologies, relevant for gate driver design.

Property	SiC MOSFET	GaN e-mode	GaN/SiC Cascode	Si IGBT[1]
Drain-source voltage v_{DS}	≥ 650V	≤ 650V	650V (GaN) ≥ 650V (SiC)	≥ 600V
On-state $v_{GS,on}$	15-20V	5-6V	10-12V	12-15V
Off-state $v_{GS,off}$	-5V-0V	-3V…0V	0V	-5V..0V
v_{GS} limits	-10…-5V +20…23V	-6V +7V	+-20V	+-20V
Threshold voltage v_{th} at 25°C	2.5-4.5V	1.1-1.7V	4V	4V
Common-mode transient immunity (CMTI)	>100V/ns	>100V/ns	>100V/ns	<50V/ns
Undervoltage lockout (UVLO)	12V	<5V	8V	12V
Charge ratio Q_{GD} / Q_{GS}	1-3	1-4	0.4-0.8	-
Gate drive supply power	medium	lowest	low	high

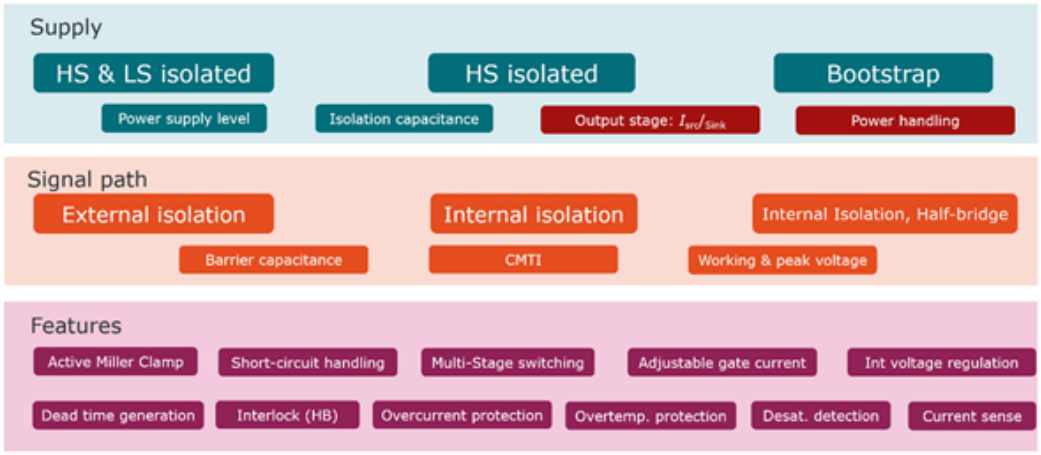

Figure 4-3: Overview of gate driver properties and features.

4.2.1 Gate Drive Power Supply

In comparison to the Si IGBT, all of the wide bandgap semiconductors can switch at very high speeds and thus require gate drive supplies that can handle rapid voltage transitions of 50-100 V/ns and beyond without introducing excessive interference into the low-voltage side

[1] For IGBTs the source is replaced by the emitter and the drain by the collector, i.e., VDS□VCE, VGS□VGE…

through their coupling capacitance. At the required power levels of only a few watts, isolated converters are often based on the low-cost flyback or push-pull topology and various integrated solutions specialized for the most common wide-bandgap voltage supply levels are commercially available with coupling capacitance as low as <3 pF. As shown in Table 4-2, the voltage level requirements differ significantly between the different device types. Most SiC MOSFETs and e-mode GaN FETs require tightly regulated positive and negative gate supply voltage for lowest $R_{DS(on)}$ as well as to prevent parasitic turn-on from unfavourable charge balance levels Q_{GD} / Q_{GS} > 1. This is especially important since there is typically only low margin between the operational voltages and the maximum permissible gate voltage. Devices based on the Cascode structure can be designed to be virtually immune against parasitic turn-on when turned off at 0V and in addition, due to being driven by a low-voltage silicon MOSFET, they achieve minimum $R_{DS(on)}$ at a wider range of 8-12V. These relaxed gate supply requirements facilitate use of a simple and low-cost unregulated bootstrap supply on the high-side. The bootstrap circuit consists only of a buffer capacitor, current limiting resistor and a fast, low-capacitance high-voltage diode with same voltage rating as the power transistors. This structure can help to significantly reduce component count of the gate driver, but it is only suitable for applications that don't require unity duty cycle or possess auxiliary circuits with high power demand.

On the output side of the gate driver, the relevant parameters that determine the driving strength are the source and sink capability as well as the internal pull-up and pull down-resistances. The maximum current capability is mainly determined by the size of the transistors of the gate driver's output stage. For very large SiC MOSFETs or several devices in parallel, peak currents of well above 10A might be required to achieve sufficient switching speed. Low internal driver resistance helps to limit the power dissipation in each of the switching cycles and leaves room for converter optimization towards higher switching frequencies if needed. On top of that, a low impedance pull-down path is vital for devices that possess high Q_{GD}/Q_{GS} ratio, as it supports extraction of the gate-drain charge from the device if low turn-off resistance is used to prevent parasitic turn-on. This is particularly important for e-mode GaN FETs due to their low threshold voltage. In cases where higher turn-off resistance is needed, an active miller clamp capability might be necessary.

4.2.2 Signal Path

Similar as described in the power supply segment, the gate signals must also be transmitted to the low- and high-side transistor without unwanted signal interference in an environment of high dv/dt. State-of-the-art isolators achieve galvanic isolation by transmitting the digital gate input signal via either opto-couplers, through a capacitive barrier or via magnetic coupling [C]. All the approaches can reach common-mode transient immunity (CMTI) of more than 100 V/ns, suitable for use with wide bandgap devices in most applications. The isolation can be provided in separate ICs with a single or several channels or might be directly integrated into single or half-bridge gate driver ICs. The high CMTI value ensures that no glitches or false triggers are introduced during the voltage transition. The isolation barrier capacitance can be as low as 1 pF and it very important to ensure that no extra coupling is introduced on the gate driver PCB design.

Isolated gate drivers are tested to withstand very high voltage peaks to ensure that the galvanic isolation barrier will be able to survive single event surge pulses in an application. For continuous operation, the maximum working insulation voltage must be considered carefully to minimize the failure rate over the lifetime of the converter. While many modern gate drivers

for wide bandgap devices can switch SiC devices at 1 kV and beyond, not all have sufficient continuous working insulation voltage rating to be reliably used in a product at very high voltage.

4.2.3 Advanced Features

In the simplest form, an isolated gate driver will only need pins for the power supply on the primary and secondary side as well as a single digital input and power output pin. Nearly all drivers also possess routines to shut down in a controlled way (under-voltage lockout) in case of insufficient supply voltage during start-up and operation or when temperature or current ratings of the gate driver are exceeded. On top of these very fundamental self-protection features, modern gate drivers can include several extra capabilities that help to increase the reliability and performance of the attached power transistors.

In single gate drivers, several solutions are typically added to the basic gate-driving functionality to improve switching performance. One of the most common is the possibility to have *separate pins for turn-on and turn-off*. This makes the device able to directly drive two separate on and off gate resistors to optimize the switching, without the need of an external diode, easing the layout.

Few drivers available on the market are proposing some interesting features to improve switching even further: *multi-stage switching* and *adjustable gate current*. Both solutions are aiming at controlling the different phases of the transistor commutation, reducing the time devoted to the Miller plateau, or reducing the effect of voltage overshoots during switch-off.

Another functionality typically present in gate drivers is the so-called *active miller clamp* (AMC). It consists in a low impedance path driven when the gate has been switched off that forces one output to the off-gate voltage level (i.e., the V_{SS}/V_{EE} rail). This directly connected to the gate of the power device reduces the effect of unwanted turn-on when high dV/dt present on the transistor output induce a current towards the gate by means of capacitive couplings (i.e., C_{GD}). This current on gate resistors can increase the gate voltage above the threshold, making risking in direct paths between power rails.

Not only performances are pursued from gate driver manufacturers, safety and reliability are key in many applications, especially in the automotive and the aerospace domains. *Short circuit protection* is one of these features: A pin of the chip has to be connected to the drain (or collector) pin of the transistor to monitor the voltage during after the switch-on completion. If this voltage is above a given threshold, it means the device is not behaving correctly either because it has been damaged, or the expected output current has been exceeded (due to short circuit or some issue in the control). In any case, the transistor has to be switched off in a safe way and prevented to switch again for a given time (to allow the extraction of the overheat generated by the high current). Since this feature has been originally developed for IGBTs and the aim was to prevent the device to exit from the saturation region, it is often named as “de-sat” pin. It has to be noticed that this is one feature that depends on the transistor technology chosen, indeed the voltage used as threshold for IGBTs is very unlikely to be the same suitable for MOSFETs, hence careful selection of the driver has to be done to make this functionality actually working in the final application. In some cases, it is possible to add some output circuitry to adapt the threshold to the desired value, but timings are crucial: If on IGBTs switching off in 10us can be tolerated, on SiC MOSFETs these values are at least halved, and in GaN HEMT it’s even shorter, making really hard to switch off the device in time if the driver is not integrated in the power transistor substrate.

In case of double gate drivers some extra features can be added to improve safety when switching a half-bridge. Indeed, the presence of both high-side and low-side drivers on the same chip makes easy forcing some degree of mutual exclusion between them. The most common solution is to grant an interlock between the drivers, forcing a minimum dead-time between the two. In more complex (and expensive) drivers, the dead-time can be configured either by programming a memory inside the device or by changing an external resistor.

Even if not very common, few drivers integrate some functionalities for voltage regulation. Some integrate a diode, necessary in case of boot-strap voltage supply techniques. Others, instead integrate a MOSFET to be used in case a DC-DC converter is used to supply the device. Both solutions are useful to reduce the area occupied on the PCB making designs more compact.

4.3 Main Parasitics in the Gate Driver

Due to the increased switching slopes of modern FETs, special attention must also be paid to minimizing circuit parasitics by choosing low inductance packaging technology and by employing routing techniques that minimize loop inductances and stray capacitances in sensitive areas. Figure 4-4 gives an overview of selected gate loop parasitics that can quickly deteriorate performance of a converter if not addressed properly in the design phase of the gate driver:

- Introducing the power source inductance L_s in the gate loop as common source inductance (CSI) should always be avoided if possible. The induced voltage during the high di/dt phase of the switching transition will act against the driving voltage of the gate driver. This will slow the switching transition and increase switching losses significantly, especially towards high power levels. In addition, it can even be a source for instability. The best way to achieve low CSI in converter design is use of a dedicated Kelvin Source (KS) pin. However, even the presence of a KS connection does not fully eliminate CSI, and the minimization effort should already start during the design phase of the chip and the package [18], [19].
- Minimization of unwanted gate to drain capacitance is another very important aspect to achieve good gate drive performance. Modern power devices are optimized for high switching speed and low total gate charge but often come with a non-optimal charge ratio Q_{gd}/Q_{gs} >1. Adding extra charge between gate-drain, for example through overlapping layers on a gate drive PCB, can reduce the switching performance significantly and might increase risk of parasitic turn-on.
- Gate loop inductance L_g should also be kept low by employing flux-cancellation layout techniques, especially when very low gate resistance R_g is used. High gate inductance will not only increase the switching delay times but it will also worsen overshoot and ringing significantly on the gate.

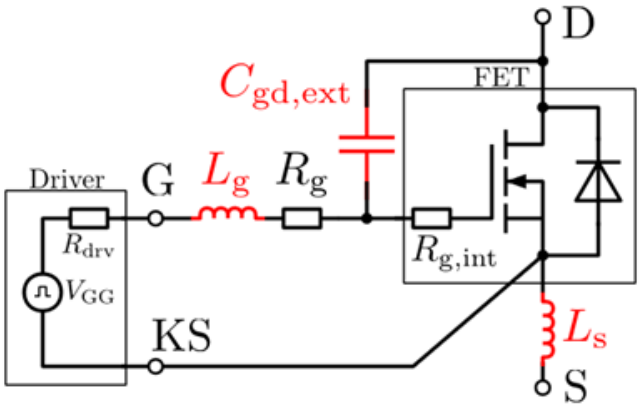

Figure 4-4: Basic gate driver circuit with parasitics (red).

While these parasitics can be kept low in a discrete setup, integration of the power semiconductors and the gate drive circuit can help to further minimize their impact and it enables the implementation of further functionality for improved performance, reliability and safety into the unit.

5. Packaging

The way power devices are packaged and connected to the rest of the world is not negligible, since the electrical stray parameters are crucial to understand the behaviour of every component. Moreover, the ability of substrates and housing to extract heat efficiently is key to build efficient and reliable systems. This chapter is providing an overview on substrate possibilities and their characteristics to enable a cost-to-performance comparison.

5.1 Substrates for Power Electronics

A substrate suitable for power electronics applications shall be able to either

- Handle high current levels (from 10 A to 1000 A), or
- Operate correctly even if exposed to high temperatures (around or above 100° C), or
- Guarantee the required insulation needed by the operating class voltage, or
- Dissipate heat effectively.

In many applications multiple of the requirements above are present, increasing the challenges in the design. Following sections are describing the technologies commercially available for power electronics with their advantages and drawbacks.

5.1.1 Printed-Circuit Boards

Printed circuit boards are the most common substrate for electronics, since they are inexpensive and reliable for many applications. Unfortunately, conventional technology is not perfectly suitable for power applications for several reasons:

• The typical copper thickness (35 um) is perfectly handling electrical signals used in data processing and acquisition systems, but when exposed to high currents traces are requested to widen too much as show in Figure 5-1.

- Standard FR4 (flame-retardant no. 4, the baseline insulator for commercial PCB application) has glass-transition point at 130° C [20], hence above this temperature the insulation between copper layers is losing its mechanical properties, making unreliable the behaviour of the whole PCB.
- Thermal properties of copper are outstanding, but each pair of conductive layers is separated by an FR4 layer, whose thermal conductivity is very small (between 0.1 W/(m ·K) and 0.5 W/(m K)), hence the heat extraction from a standard PCB can be cumbersome.

Two main countermeasures can be used to overcome these limitations, i.e., heavy-copper, high TG materials, and thermal via-hole technology holes [21].

5.1.1.1 Heavy-Copper Technology

Thick-copper or heavy-copper PCB are circuit boards where the copper foil is thicker than standard (35 um also known as 1 oz). This is done to improve heat spreading and dissipation and to carry more current through the traces. The size of the copper foil is multiple of the 35um, hence 70um, 105um… For special applications it is possible to arrive up to 1-2mm [22].

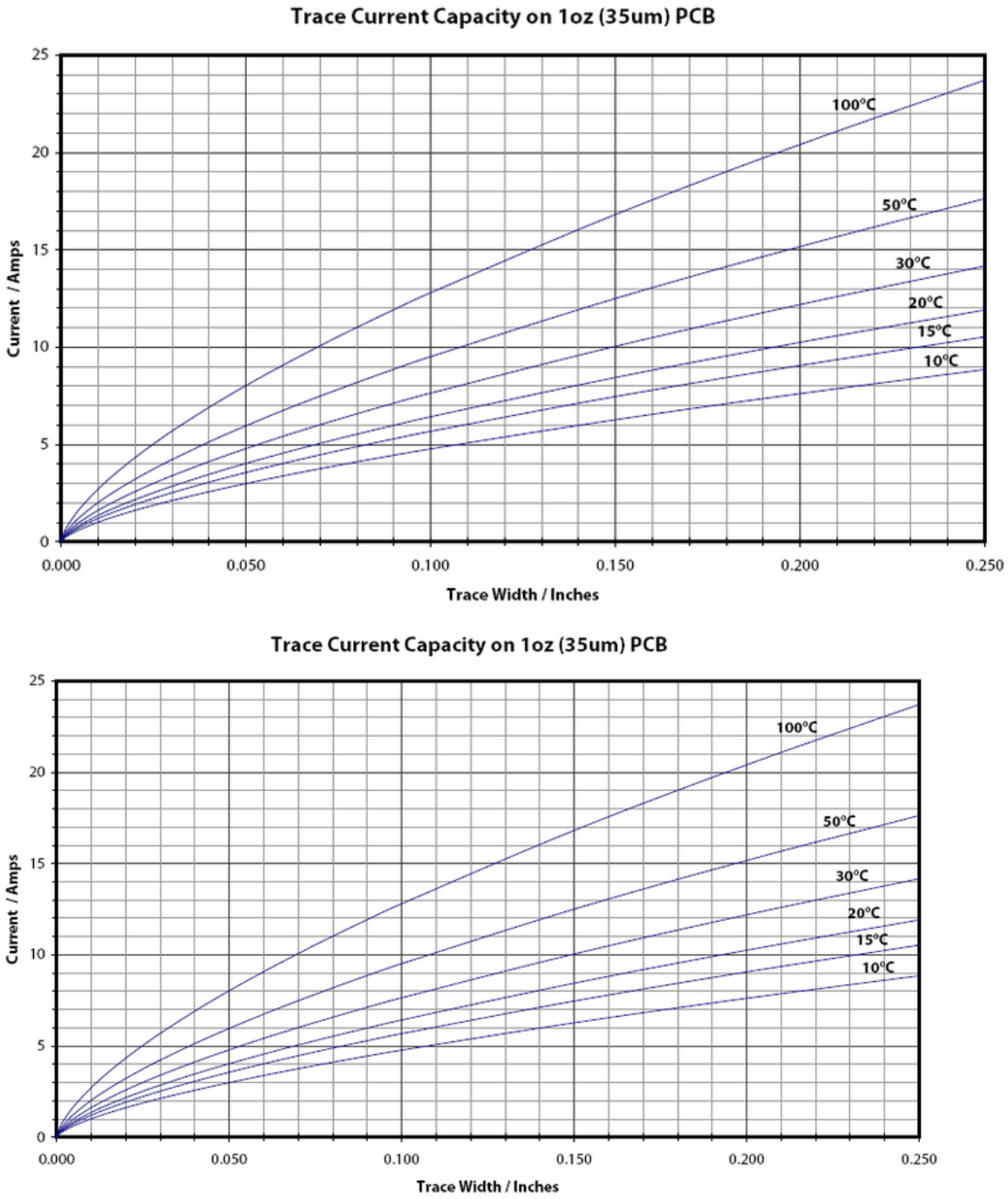

Figure 5-1: 35um copper traces ampacity according to [23].

Advantages of heavy-copper technology:

- Higher current capability: thicker traces are less resistive; hence they have lower voltage drops in case of high currents, reducing the heat generated on PCB and hence improving the thermal behaviour of the system.
- Improved heat dissipation: thermal resistance of the PCB is given by the material stack-up and on the ability each layer has to spread the heat. Using thick copper, it is possible to spread laterally the heat and hence to increment the area of dissipation.
- Increased thermal inertia of the PCB.

Drawbacks of heavy-cooper technology:

- Copper balancing on both external layers needs to be taken into account to avoid bending due to thermal cycles that will reduce substrate reliability being one cause of delamination [24].
- The manufacturing process is more complex of the one used for standard PCBs. Indeed, the presence of high thickness metal to be etched requires the usage of special lamination and etching technologies to grant high reliability in the final product [22].
- Cost, since copper is an expensive and inflated material. Moreover, above a given thickness, the process is less common, increasing costs and production time.

5.1.1.2 High Tg Material

The glass transition temperature (Tg) is the temperature at which a polymer changes from hard condition to a viscous condition, changing most of its physical properties (like hardness, coefficient of thermal expansion, specific heat…) [25]. Changes are reversible as long as the resin has not being degraded [20]. As shown in Figure 5-2, the Tg is defined as a number, but in practice it is more a transition zone, for this reason is typically safer to keep a safety margin of about 10° C from the number granted by the PCB manufacturer.

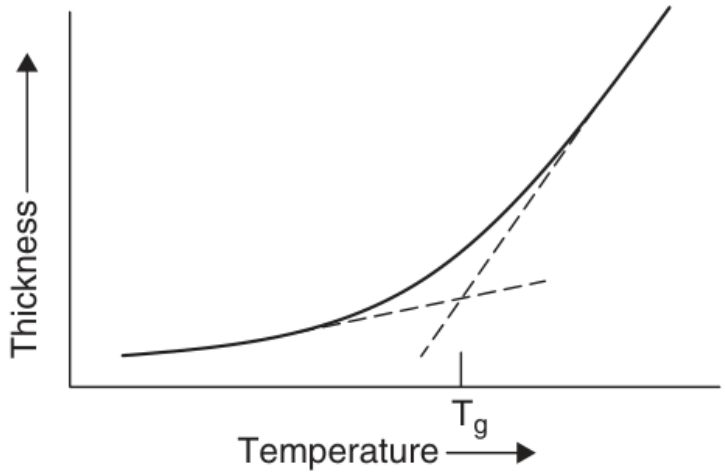

Figure 5-2: Definition of the glass transition temperature [20].

Typical FR4 materials are granted to have Tg at 130°–140° C, but this is not suitable for high temperature operations or for high current operation, where even if the global temperature stays below this value, it is possible to experience local overheating due to the joule effect.

Selecting the proper Tg for a given application is key to keep it operating in a reliable way in all working conditions, but higher Tg is not always the best solution for all the applications. Indeed, Tg can be increase by incorporating some fillers that can degrade the global CTE of the PCB. This might result in the counterintuitive effect of having higher Tg substrates with higher CTE compared to lower Tg materials. FR4 is also available with Tg around 170°–180° C. For higher temperatures there are other materials up to 260° C of Tg, among them Polyimide is one of the most known and used (i.e., in flexible circuits).

5.1.1.3 Thermal Via -Holes and Copper Coins

Standard via holes is connecting different copper layers to allow traces moving from one layer to another. Since the via is composed of a hole and a metallic barrel, it can be used to reduce the thermal resistance of the PCB. The typical approach is to insert multiple vias into thermal

pad, granting a good thermal link between the hotspot (i.e., the device to be dissipated) and the heatsink.

Thermal via holes can be realized in different ways and after contacting many PCB manufacturers [22, 26, 27], it is possible to draw these considerations (see Figure 5-3):

Tented vias, where the hole is only covered by solder mask, are the cheapest solution but do not provide any thermal improvement over standard not filled via

a) Filled and capped via (filled with non-conductive resin) provide the best trade-off, allowing via-in-pad for the lowest thermal resistance
b) Thermally conductive resin provides a negligible improvement since the copper plating dominates the conduction but increases the cost significantly
c) Copper-filled vias have the highest thermal conductance, but the process is not so common and thus it is more expensive than traditional solution

A more extreme solution is the inclusion of the so-called *copper coins* into the PCB. Instead of adding holes and then add metallization by means of a galvanic process, the copper coin is the insertion of a small copper cylinder into a PCB that has been milled to host this component. Resulting thermal properties are improved because of the metallic path between the power device to be dissipated and the heatsink, but cost increase because of the increased process complexity.

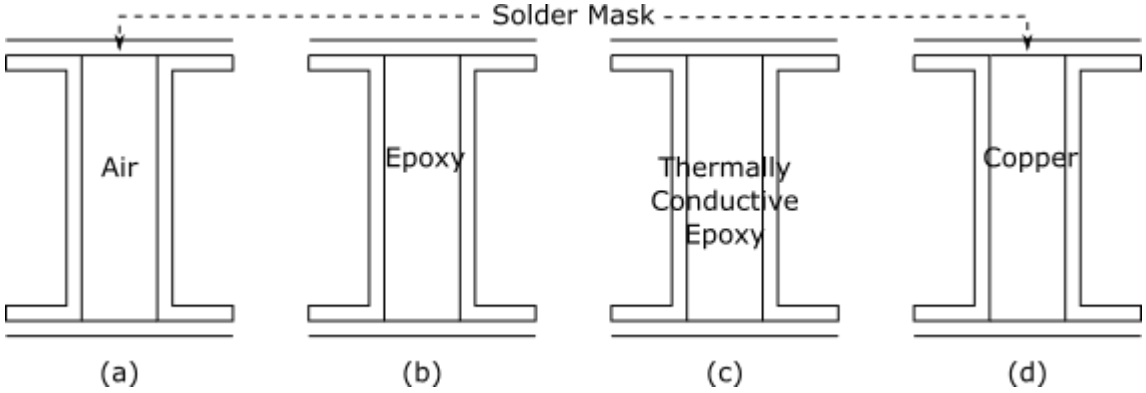

Figure 5-3: Possible via solutions.

5.1.1.4 Top-Side Cooling approach

Another way to cope with high heat extraction requirements but remaining with classical substrates is to drastically change the approach. In standard PCB-based application the substrate has to carry both high currents and dissipate heat efficiently, a constant trade-off process is addressed to avoid one aspect is jeopardizing the other. For this reason, removing one of these tasks from the substrate can lead to more optimized designs. This leads to the so-called top-side cooling approach.

The idea is simple: instead of conveying both current and heat towards the PCB, while the current still is handled by the copper into the PCB, a power pad is available on top of the chip to be dissipated, enabling the direct contact with a heatsink (Figure 5-4). This solution has the direct advantage to reduce the thermal resistance between the junction and the heatsink (since the PCB is no longer in this path), hence improving the heat transfer between the power device and the cooling element.

In the last years several manufacturers have proposed their own package version based on this approach, CCPAK1212i (Nexperia [28]), TOLT (Infineon [29]), HU3PAK (ST [30] and Wolfspeed [31])... Any manufacturer has its own strategy to propose these packages, but general consideration about their thermal performance can be made looking at [32]:

- The size of the thermal pad, especially compared to the total package area: the higher the ratio between the two, the higher the capability to dissipate heat
- The technology used for pin connection, standard bonding is cheaper, but copper clips are enabling higher heat dissipation (and are also improving stray inductance and current density).

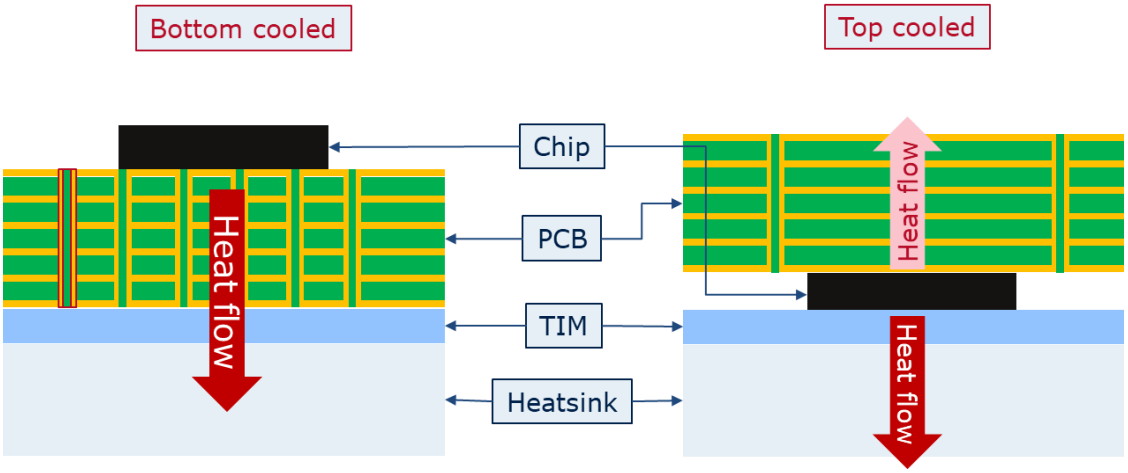

Figure 5-4: Comparison of traditional cooling through the PCB (left) and top-side cooling (right).

5.1.2 IMS – Insulated-Metal Substrates

IMS substrates are used mainly in low-cost and low-power application (i.e., LED) and are characterized by direct contact between the insulating material and the module base plate. Electrical insulation is granted by a plastic material or by a passivation layer created directly on the substrate. Once the insulation layer has been created any structure can grow on top of it; a typical solution is to attach a single/multi-layer PCB where the circuit functionality is implemented. The main advantages of IMS technology are low costs, high complexity of resulting circuit, and high mechanical substrate stability.

An IMS is composed of three parts [33]:

- A metallic substrate;
- A thermal interface material, used to electrically insulate the substrate from the circuit;
- A circuit layer where the desired layout is drawn.

The substrate is a thick foil of either copper, aluminium, or steel (in specific cases). It is used as heatsink and mechanical structure of the IMS. These substrates can have a thickness between 1.0- and 3.2-mm [22] [33]. Copper provides the highest thermal conductance (380-400 W/(m·K)) but also the highest density (ρ = 8900 kg/m^3) and the highest cost. In case either cost or weight are important, aluminium is usually chosen (ρ = 2700 kg/m^3, λ = 180 W/(m·K)). Steel is more complex to use but provides the lowest coefficient of thermal expansion among proposed metals.

Thermal interface material (TIM) in IMS is typically around 40-50 µm, i.e., five to ten times less thickness required for ceramic insulations in DBC/AMB substrates. TIM conductivity is between 1 and 12 W/(m·K). Even if these values are not as high as those used for DBC (see Sec. 5.1.3), thanks to the reduced thickness you can deposit these materials (less than 100 µm) the resulting thermal resistance is comparable to DBC with a lower cost.

Circuit layer is based on standard PCB technology and was born as single layer. Nowadays it is easy to find also dual and quad layer structures, obviously this makes a trade-off between circuit complexity and thermal properties. Copper thickness can vary, depending on what the application requires. Copper foils can grow up to 500 µm.

5.1.3 Ceramic Substrates

Ceramic substrates are key materials in the electronics industry due to their combination of mechanical, thermal, and electrical properties. These materials are widely used to support electronic circuits, dissipate heat, and provide electrical insulation.

Ceramic packaging solutions deliver exceptional reliability compared to organic technologies and incur significantly lower development costs than those needed for monolithic semiconductor integration. The use of ceramic substrate technologies in microelectronics is driven by factors such as system-in-package integration capabilities, efficient thermal management, resistance to high temperatures, and the ability to integrate heterogeneous systems with varying thermal expansion coefficients.

Ceramic substrates offer the distinct advantage of having thermal expansion coefficients that closely match that of silicon. In contrast, the thermal expansion of IMS (Insulated Metal Substrate) is dictated by the base plate material—either copper or aluminium. This can lead to significant stress between the substrate and the silicon chip during temperature fluctuations. As the industry shifts towards higher voltage ranges, Insulated Gate Bipolar Transistor (IGBT) modules face increased demands for high insulation voltages and exceptional partial discharge stability. These attributes depend on various factors, including the thickness, material, and uniformity of the chip's bottom insulation, as well as the module's casing and filling materials. Moreover, sometimes the arrangement of the chips also plays a role. Modern transistor modules undergo rigorous insulation testing, with test voltages ranging from 2.5 kV to 9 kV, and each module is verified for compliance during production.

In the realm of electronics, ceramic substrates are typically identified as "ceramic printed boards" or more accurately, as part of film integrated circuits. They are extensively utilized in microelectronic packaging, sensor and actuator technology, and passive component production. The most common substrate type is the flat, rectangular standard thick-film substrate made from 96% alumina, created through tape casting and fired at high temperatures around 1600°C.

In addition to these, substrates made from 99% alumina for thin-film applications, zirconia-stabilized alumina, and aluminium nitride are also employed in thick-film and thin-film technologies. Moreover, specific forms and shapes are crafted for specialized applications, such as pressure sensors, heating elements, and micro-cooling units. These specialized pieces are generally dry-pressed or extruded and then fired at 1600°C, with thick-film processes adapted to their particular forms.

Unlike standard single or double-sided substrates, the processing of ceramic multilayer substrates and packages involves a different approach. Many thick-film processes are applied

to unfired, or "green," ceramic sheets made via tape casting. After these sheets are metallized with refractory metal inks for high-temperature co-fired ceramics (HTCC) or noble metal inks for low-temperature co-fired ceramics (LTCC), they are stacked, laminated, and co-fired. The high temperature process at 1600°C yields HTCC, while the lower temperature process at 850°C results in LTCC. Manufacturing processes must be tailored to the unique requirements of green ceramics. These technologies enable high integration density and significant miniaturization, while also offering excellent reliability.

5.1.4 Direct Bonded Copper (DBC) and Active Metal Brazing (AMB)

Direct Bonded Copper (DBC) and Active Metal Brazing (AMB) are advanced technologies employing a thin ceramic insulator covered with metallic layers on both sides. These substrates are crucial for applications requiring both high mechanical support and efficient thermal management.

5.1.4.1 Direct Bonded Copper (DBC)

In DBC technology, a ceramic insulator is bonded on both sides with copper layers through a precise, controlled thermal process. This technique provides a strong, reliable bond without the need for additional bonding materials, making it ideal for applications with stringent thermal and mechanical demands. Its compatibility with silicon's thermal expansion coefficient reduces stress on semiconductor devices, enhancing longevity and performance stability, particularly important in high-voltage applications like IGBT modules.

5.1.4.2 Active Metal Brazing (AMB)

AMB differentiates itself by using a brazing paste during bonding, requiring a vacuum environment during the welding process. This method allows for adaptability in production and material composition, often chosen for its flexibility in manufacturing environments where precise control of bonding conditions is necessary.

Both DBC and AMB share similar post-production characteristics, exhibiting consistent wire bonding, welding properties, and analogous thermal behaviour, which positions them as leading solutions in high-power electronics.

These substrate technologies, when combined with materials like aluminium nitride, enhance their thermal management capabilities, marking them as pivotal components in expanding fields such as power electronics and energy management.

5.1.5 PCB Embedding

In the recent years PCB manufacturers started proposing the approach to embed devices in the substrate to reduce at its minimum the stray parameters introduced by chip packages and to improve thermal resistance towards the heatsink [34]. Another important advantage is given by the total assembled cost, since reduces the assembly process, moving part of this complexity in another production phase [20].

It is possible to integrate both passive and active components in the substrate, obviously with different processes (Figure 5-5). Passive components can be either formed by deposing a material with proper characteristics between terminals or inserted (i.e., starting from existing chips). Active components instead can only be inserted in the lamination process.

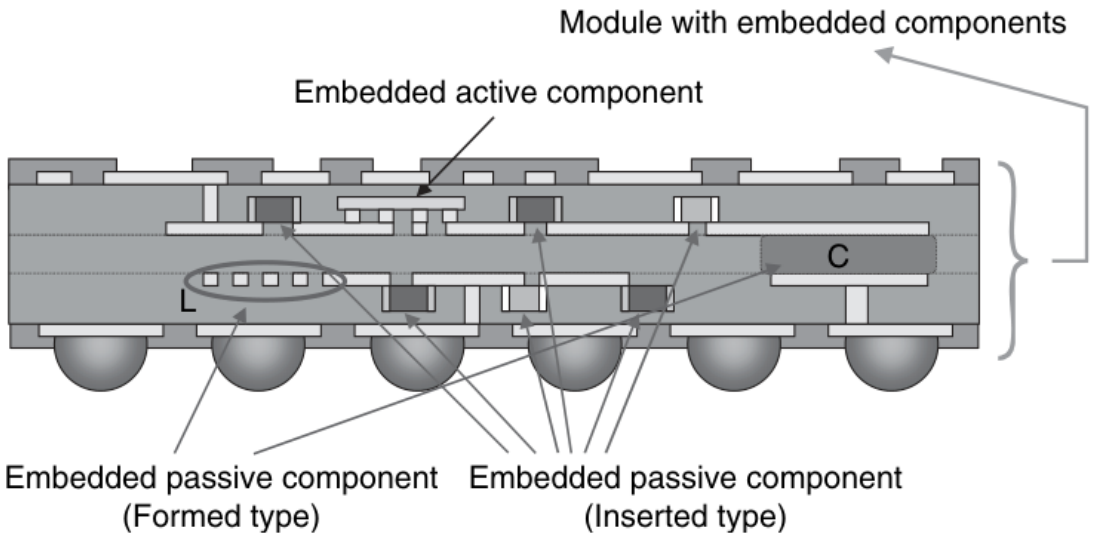

Figure 5-5: Cross section of a multilayer board showing the use of all types of embedded components [20].

Advantages of the embedding process:

- Improved design density, since components usually occupying the outer layers are integrated in the substrate, freeing space for other devices.
- Reduction of stray elements introduced by packaging and distance, given by the shorter interconnection between parts and the removal of the outer package (effective to improve the switching capabilities of WBG devices).
- Reduction of the total costs of assembly, reducing both the bill of materials and the assembly time.
- Improve heat dissipation, given by a higher capability of spreading heat thanks to the surrounding copper layers and the lower junction to heatsink thermal path (thermal conductivity of PCB embedded can reach the value of ceramic substrates [35] [36]).

Disadvantages of the process:

- Quality of the process is reduced, since it requires more steps and CTEs of the chips might be different from the one of the substrate (situation typically relaxed by the presence of leaded packages in conventional assembly).
- Cost of prototypes can be higher due to the more complex process that is not split on a whole production.
- Reworks are not possible inside the board.

5.1.6 Substrate Comparison

Following few considerations about reliability and thermal performance of the substrates described in previous sections.

5.1.6.1 Thermal Conductivity

The substrates described in previous sections have different thermal performance and thus costs. Figure 5-6 provides a graphical comparison amongst these substrates for converters in the range of 30kVA [37]: As expected, ceramic packages are the most efficient to extract heat,

providing a very low junction-to-heatsink thermal resistance. IMS is following if considering typical processes and standard FR4 PCBs are less performing. These are general considerations, and they depend on the actual implementations (materials used, stack-up). As general considerations, they can be wrong is particular cases, as the one discussed below.

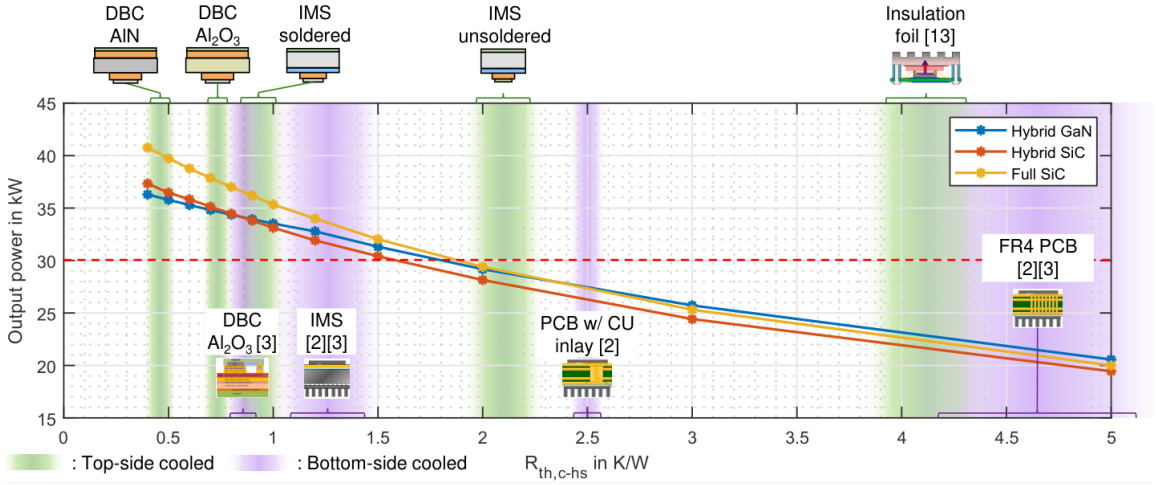

Figure 5-6: Comparison of thermal performances of different substrates [37]. (References shown in this picture are those of the original publication.)

Table 5-1 reports thermal conductivities and thermal expansion characteristics of different types of substrates commonly used for power electronics application. The three families shown are PCB, IMS, and DBC/AMB. For each of them several configurations are reported. It is easy to see how characteristics can widely change within the same family. Indeed, their peculiarities are tightly related to the materials used in all the layers. Let us take:

- A PCB with total thickness of 0.65 mm, with 4 layers, each of them composed by 70 µm copper, and filled vias (i.e., in specific areas of the PCB thermal dissipation is improved by metallized holes (vias) that are filled with a conductive paste);
- An IMS with Aluminium substrate 1 mm thick, insulated by a filler with thermal conductivity of 2 W/(m·K).

Combining data from Table 5-1 with thicknesses above and calculating the thermal resistance of the two substrates in example, it is possible to obtain the results of Table 5-2: The two substrates provide very similar thermal performances. Indeed, the comparison is between a high-performance PCB process with a poor IMS one. Moreover, the PCB is composed of 4 routing layers, whilst the IMS taken into consideration has only one. Moving to an IMS process with two or four routing layers, the overall thermal resistance will increase and thus the benefit of IMS would reduce even further. Another very important point is cost, indeed reduced thickness and filled-and-capped vias are non-standard and hence increase PCB cost.

Table 5-1: Thermal conductivity and coefficient of thermal expansion of PCB, ISM, and DBC.

Substrate	Thermal conductivity, W/(m·K)	CTE, ppm/K	Notes
PCB (35-µm Cu)	0.3	13-16	2-layer, 1.6 mm
PCB (70-µm Cu)	0.5	20-25	4-layer, 0.65 mm
PCB (70-µm Cu + vias)	7.0	20-25	4 layers, 0.65 mm, 90 vias/cm^2
DBC/AMB – AlN	180	5.7	300 µm insulation
DBC/AMB – Al_2O_3	24	8.3	
DBC/AMB – AlSiC	150 ÷ 180	7÷10	
IMS fillers (TIM)	1.0 ÷ 12	Selected to match substrate	30 µm insulation (min), aluminium substrate
Copper	390	17	Used as substrate for IMS
Aluminium	150 ÷ 180	25	
Steel	50	13	
Silicon	130	2.6	
Silicon Carbide	120	4.0	
Silicon Nitride	30	3.3	

Another good example can be done comparing IMS and DBC:

- A leading-edge IMS process with very performant TIM (6 W/(m·K)), 30 µm thick and copper substrate;
- A DBC based on aluminium oxide (Al_2O_3), 300 µm thick.

Performing the same analysis did for the previous case, we can see that the IMS chosen is outperforming DBC (Table 5-3).

Concluding there is not a golden rule that states which substrate is better, but it is a game of trade-offs. Each application is different, and considerations must be made to have a clear picture about the benefits and the drawbacks different technologies provide.

Table 5-2: Comparison of thermal characteristics of a cheap IMS process and an expensive PCB one.

		Lambda	Thickness	Area	Rth
		W/m/K	mm	mm2	K/W
IMS	Conductors (Cu)	390	0.070	100	1.8E-3
	TIM	2	0.150	100	750.0E-3
	Substrate (Al)	180	1.000	100	55.6E-3
					807.4E-3

		Lambda	Thickness	Area	Rth
		W/m/K	mm	mm^2	K/W
PCB	PCB with filled vias	7	0.65	100	928.6E-3
					928.6E-3

Table 5-3: Comparison of thermal properties of a cheap DBC process and an expensive IMS one.

		Lambda	Thickness	Area	Rth
		W/m/K	mm	mm^2	K/W
IMS	Conductors (Cu)	390	0.070	100	1.8E-3
	TIM	6	0.030	100	50.0E-3
	Substrate (Al)	180	1.000	100	55.6E-3
					107.4E-3

		Lambda	Thickness	Area	Rth
		W/m/K	mm	mm^2	K/W
DBC	Al_2O_3	24	0.3	100	125.0E-3
					125.0E-3

5.1.6.2 Considerations on Reliability

All substrates described so far are based on laminated materials, but while PCB is composed by a stack of copper layers, separated by glass-fibre ones, hence a uniform structure, both IMS and DBC/AMB are more heterogeneous. Obviously, thermal performance is different and sections above detail which are the consideration to made to decide the best material as substrate. What has not been mentioned so far and is forgotten often is the mechanics of these objects. Indeed, they are not static objects that are immutable in all usage condition. The focus is on the interaction among materials with different CTEs.

Looking at IMS, using aluminium as base and copper for conductors generates stresses at the interface. Especially when the thickness of conductor layer becomes comparable to the base (above 10% of its thickness [38]), not only stresses are high and might affect overall reliability when the board is exposed to thermal cycling, but ensuring flatness of the board might be

cumbersome. This might modify thermal performance, especially when the board has to be interfaced with a cooling surface.

Another aspect related to CTE is how thermal stresses are transmitted to components. Indeed, most components have been designed for PCB applications, where CTE is limited to copper dilatation at high temperature (CTE_{Cu} = 17 ppm/K), whilst on IMS, it is the base leading thermal expansion (CTE_{Al} = 25 ppm/K in case of aluminium). This particularly mines reliability of large components in case of wide temperature ranges. IMS requires special care for component selection, in order to avoid elevated tensions on welding joints on the devices mounted on top of it.

Table 5-4: Comparison between AMB and DBC [39].

Ceramic	Bonding	Conductor	Plating	0-350° C Thermal Cycles [39]
AlN, 0.6mm	DBC	Cu, 0.3mm	ENIG	12
Al_2O_3, 0.4mm	DBC	Cu, 0.3mm	Ni-P	13
Si_3N_4, 0.3mm	DBC	Cu, 0.3mm	None	124
Si_3N_4, 0.3mm	AMB	Cu, 0.5mm	None	145
Si_3N_4, 0.3mm	AMB	Cu, 0.5mm	ENIG	450
AlN, 0.6mm	AMB	Al, 0.4mm	Ni-P	990

Copper has its own drawbacks, mainly related to costs (the bar metal cost more and it requires more processes to be used and to be passivated). An appealing alternative is aluminium silicon carbide (AlSiC), that can be produced to have various CTE (Table 5-1) to be suitable to host to different materials, from silicon devices to SiC [40], reducing mechanical stresses, and not needing expensive passivation processes.

With respect to DBC/AMB, the importance of the selected substrate results in power module reliability and endurance when exposed to thermal cycles. In [39] are described extreme thermal cycles, from 0 to 350° C, used to characterize and compare a set of different materials and configurations (see Table 5-4). The first five columns are directly taken from [39],

Looking deeper to the results described above, what immediately emerge is how the stack of materials composing the DBC/AMB substrate directly impacts the overall reliability of the object. The more the base material and the ceramic differs in CTE value, the greater the mechanical stresses in the structure, thing that results in reduced lifetime in case of wide thermal excursion.

5.2 Finishing of Surfaces

Exposed copper will naturally oxide and loose its capacity to weld. Surface finishing of PCBs aims at creating a protective layer that helps preserving copper in perfect conditions to allow welding.

Finishing is a layer of material that avoid the copper to be attacked by external oxidation agents but must be thin to let the welding process make the solder joint on the copper.

Finishing thickness will directly affect the shelf life of these components, i.e., the time for whom the surface properties are guaranteed and hence the time frame in which the PCB assembly shall be completed, in order to have maximum reliability. Indeed, when two metals are jointed,

an intermetallic layer can form. This layer naturally migrates to the surface of the joint, given enough time. When the intermetallic reaches the surface, solderability of the surface is no longer guarantee: This is where shelf-life comes from. Having a thick finishing surface automatically increases the shelf life, since the time required to the intermetallic layer to arrive to the surface is longer.

Following some characteristics of the most used technologies:

- Hot-air solder levering (HASL/HAL), is one of the oldest and cheapest finishing processes, the PCB is immerged into molten solder and then passed through air blades to remove excess of material. Resulting finishing layer is pretty thick, can be reworked many times, but it is not suitable for fine-pitch and when high planarity is required. It is not suitable both for sintering and for wire bonding.
- Electron-less nickel gold plating (ENIG) is a process that exploits gold properties, i.e., it does not form oxides and it dissolves inside solder, making it suitable for perfect solder joints. It is expensive and if gold quantity exceeds 3% of weight of the solder can produce brittle solder joints. Moreover, it tends to mix with copper, hence a thick layer of nickel is interposed between pads and the gold protective layer. The process generates stress on the PCB because it is at high temperature and endures for long time (about 40-50 minutes at 90° C). It is suitable for wire bonding (Al), but not suitable for sintering processes.
- Immersion silver uses this precious metal as protecting surface. Silver is the metal with lowest conduction and contact resistance, hence it is perfectly suitable for joints. It is more resistant to oxidation, compared to other metals, but not as much as gold. The forming process is simpler and dwell time is reduced to few minutes at low temperature (50° C). It is suitable for wire bonding (Al and Au) and suitable for sintering processes.
- Immersion tin guarantees good solderability, but it forms rapidly intermetallic with copper, affecting shelf life. It is very cheap. It is not suitable both for sintering and for wire bonding.
- Organic solderability preservative (OSP) technology uses thin organic layer to preserve copper surface from oxidation. It is the cheapest process, but it is less resistant to mishandling. The process is simple, and the dwell time is short, reducing at most the stresses on the PCB. Solder joints done on this finishing are typically mechanically more resistant and more stable.
- Electroless palladium is an alternative to ENIG with similar costs. It is suitable for wire bonding (Al and Au) and suitable for sintering processes.

Table 5-5 summarizes important characteristics for different finishing technologies.

Table 5-5: Characteristics of surface finishing normally used [20].

Finishing	Thickness, (µm)	Planarity	Shelf-Life (months)	Cost
HAL	2÷40	poor	18	Cheap
ENIG	3÷5 (Ni), 0.05÷0.15 (Au)	good	24	Expensive
Immersion silver	0.1÷0.04	good	12	Cheap
Immersion tin	0.6÷1.2	good	6	Cheap
OSP	0.1÷0.6	good	6	Cheap
Electroless Palladium	4÷7 (Ni), 0.05÷0.25 (Pd)	good	24	Expensive

For ceramic substrates instead there are various finishing options that can be applied based on the requirements of the application. Here are some of the most common:

- Metallization: This involves applying a conductive metal layer, such as copper, gold, silver, or platinum. This finish is essential for creating circuits and connecting electronic components.
- Glass Coating: Used to provide chemical and mechanical protection to the underlying substrate. It also helps improve resistance to high temperatures and chemical influences.
- Nickel Plating: This involves depositing a layer of nickel on the ceramic substrate's surface, enhancing oxidation resistance and solderability.
- Tin Plating: Applying a layer of tin offers excellent soldering properties and is often used to improve electronic connections.
- Gold Plating: Provides high electrical conductivity and corrosion resistance, making it a common choice for high-reliability applications.
- Lapping or Polishing: These processes are used to achieve a very smooth surface and improve the substrate’s flatness, which is important for high-precision integrations.
- Layering with Dielectric Materials: For some applications, dielectric layers may be added to modify the substrate's electrical properties.

The choice of finish depends on the functional, environmental, and cost specifications of the project where the ceramic substrate will be used.

When comparing the plating processes for ceramics and PCBs, it's crucial to recognize that both need to effectively enable electrical connectivity and durability, but the underlying material properties and end-use applications heavily influence how these goals are achieved. Ceramic substrates are typically more robust and thermally stable than the materials used for PCBs. This influences not only the choice of plating materials but also the methodologies employed. Ceramics can endure harsher chemical environments and higher processing temperatures, whereas PCBs, more susceptible to chemical interactions, require gentler treatments.

The function of each component greatly affects the plating process. Ceramic substrates may be used in environments demanding extreme thermal or mechanical performance, influencing decisions on the thickness and type of plating metals. In contrast, PCBs often prioritize miniaturization and feature density, driving innovations in patterning and finishing techniques to maximize circuit functionality within limited spaces.

Several similarities and differences emerge by the process point of view; both ceramics and PCBs require thorough surface preparation to ensure effective adhesion of the plating material. They typically begin with an electro-less plating step, often using copper, to establish a conductive base layer on non-conductive surfaces. Following this, both types of substrates undergo electroplating to increase thickness, conductivity, and durability, utilizing common metals such as copper, nickel, and gold, depending on desired properties like conductivity and corrosion resistance.

Despite these similarities, there are key differences in their processes. Ceramic substrates and PCBs have fundamentally different base materials, influencing the specific chemicals and techniques utilized during plating. Regarding final finishing, PCBs often entail soldermask application and silkscreen printing to protect circuitry and guide assembly, whereas ceramic substrates might not need these processes unless used in similar circuit-based applications. Thermal considerations also differ; ceramics often require processing that can withstand high temperatures due to their common use in high-power applications, whereas PCBs are designed with distinct thermal management requirements. Understanding these similarities and differences is crucial for selecting the appropriate processes based on the specific application requirements and substrate materials.

5.3 Multilayer Substrates: HTCC and LTCC

Traditional single and double-sided ceramic substrates often fall short in terms of integration density, miniaturization, RF performance, and system-in-package capabilities. While standard HTCC (High-Temperature Cofired Ceramic) multilayer packages have been available for over two decades – primarily produced by major Japanese companies – customized HTCC solutions are gaining traction in RF housing and microsystem integration.

Commonly, alumina is used in HTCC production, which can be either white or black, and the metallization involves refractory metal powders such as tungsten, manganese, and molybdenum. For connectivity between the chip and board, wire bonding and solder surfaces are plated. Due to the high sintering temperature, the choice of metal conductor materials is limited (mainly tungsten, molybdenum, manganese and other metals with a high melting point but poor electrical conductivity). The production cost of the high-temperature co-fired ceramic substrate is high, and its thermal conductivity is generally in the 20 ~ 200 W/(m•℃) (depending on the ceramic powder composition and purity).

In recent years, Japanese manufacturers have also introduced LTCC (Low-Temperature Cofired Ceramic) multilayer packages for RF applications, and more recently, aluminium nitride multilayer packages have become available. These suppliers use proprietary materials, controlling the entire process from powder preparation to tape casting and plating, which necessitates large production volumes to keep manufacturing lines running efficiently. Due to the lower temperature co-firing (sintering temperature to 850 ~ 900 ℃) gold and silver with good conductivity can be used as electrodes and wiring materials.

Conversely, LTCC substrates present a different scenario. Well-established "green tape" systems are readily available from reputable thick-film suppliers. The specialized knowledge

in LTCC technology, coupled with application expertise, forms the foundation for small to medium-sized European LTCC foundries allowing them to serve the open market with great flexibility in medium to low volumes. These facilities offer free sintering along with co-fired and post-fired metallization ready for all post-processing techniques (soldering, brazing, and wire bonding), complemented by a comprehensive range of resistor and dielectric inks, providing full system capabilities without additional processing.

While major players in Japan focus on high-volume markets, other companies mainly address captive markets within the automotive and telecom industries, relying on their proprietary materials and processes.

The technical performance and key characteristics are analysed in Table 5-6, giving a comparison of ceramic packages compared to other technologies. The figures for HTCC are based on Al_2O_3 [41].

Table 5-6: Physical characteristics of substrates [41].

Property	PCB	LTCC	HTCC	Si
Volume resistivity Ω*m @ RT	1011	1011	1011	1011
Break Down Voltage V/µm	40	>40	15	-
Thermal Coefficient of Expansion (TCE)	16	6	7	3
Flexural Strength in MPa		210	350	100
Thermal Conductivity W/(m K) (RT to 400°C)	0,1	3	20	125
Dielectric Const 1MHz	4,7	7,85	9,8	12
Dielectric Const 10GHz		7,83	9	
Integration of passive components	L	L, R, C	L	L, R, C

5.4 Thermal Interfaces Materials

In today's world of highly integrated microelectronic devices, efficiently managing heat is crucial for effective device design. One of the main challenges is ensuring rapid dissipation of the significant heat produced by tightly packed transistors to prevent thermal breakdown. Within the intricate structure of a device, various materials are used, forming numerous interfaces. Moreover, during the packaging process, additional components like heat dissipation elements are incorporated, creating interfaces between the main device and these supplementary components. These interfaces typically hinder heat transfer due to complex interactions and scattering processes. The resistance to heat transfer across these interfaces, known as interfacial thermal resistance (r_{th}), indicates how much an interface restricts heat flow. It is given by the formula:

$$r_{th} = \frac{\Delta T}{J}$$

Where ΔT represents the temperature difference between adjacent materials at an interface, and J is the heat flux density through the interface. r_{th} is measured in m² K/W, illustrating the temperature difference generated per watt of heat power passing through the interface. A lower r_{th} denotes more efficient heat transfer, while a higher r_{th} indicates less effective performance. This means that to improve the heat dissipation across an interface it is important to minimize the value of r_{th}. From a materials standpoint, this can be achieved by employing Thermal Interface Materials (TIMs) with the highest possible thermal conductivity. These specially engineered materials fill micro gaps and offset surface imperfections when electronic devices connect with heat dissipation elements. The primary aim is to reduce thermal resistance hampering heat transfer at the interface. Next sections are briefly introducing these materials but in case of further readings, please refer to [42, 43, 44].

5.4.1 Fundamental on TIMs

As device power densities escalate and miniaturization continues, managing thermal interfaces becomes increasingly critical to ensuring the performance and reliability of electronic systems. Thermal interface materials can be defined as materials that are applied between the interfaces of two components to enhance the thermal coupling between these devices. They are crucial for effective thermal management in electronics, providing vital pathways for heat transfer from components to heat sinks by reducing interfacial thermal resistance.

TIMs are typically composite materials that consist of thermally conductive fillers embedded in a polymer matrix. Fillers like aluminium oxide or boron nitride ensure high thermal conductivity, while the polymer enables easy handling and maintenance of the material's shape and phonon scattering at interfaces is addressed through structural design.

TIMs can be categorized into various types based on their characteristics and application needs:

- Liquid TIMs, that in turn can be divided in *unreactive*, such as thermal gels and thermal greases, and *reactive*, including thermal gap fillers and conductive adhesives;
- Solid TIMs, that can be *thick*, as in the case of Phase Change Materials and thermal pads, or *thin*, like thermal tapes.

Following is reported an overview of the main characteristics for the different types of TIMs belonging to both the liquid and solid categories.

- Elastomers and Pads: combine high thermal conductivity and electrical isolation into a single component offering mechanical robustness, ideal for applications requiring reliable and consistent interface contact. By integrating thermally conductive fillers, rubber interface materials benefit from higher thermal conductivity while maintaining high dielectric strength even at high temperatures.
- Gap Fillers: thermally conductive Gap Fillers are soft, malleable interface materials with high thermal conductivity, ideal for applications with significant distances between the heat source and cooling surface, varying component heights, high tolerance stack up variability, and uneven or rough surfaces. The conformability of gap fillers eliminates air between surfaces with higher conductivity materials to reduce thermal resistance. Since gap fillers are gel-like, volume stays constant and will thin and spread out with applied pressure. Gap fillers are naturally thixotropic, which improves handling during assembly.

- Greases and Gels: spreadable compounds with thermally conductive filler particles specially designed for high thermal conductivity to reduce thermal interface resistance between surfaces. Thermal greases are popular thermal interface material choice for many high-performance thermal management applications. When two flat surfaces are mated together with grease, the grease spreads out and thins, decreasing the thermal resistance between surfaces. However, while providing low thermal resistance and easy application they may suffer from pump-out and dry-out issues over time.
- Phase Change Materials (PCMs): PCMs are thin wax-like materials designed to melt from solid to liquid at operating temperatures to fill interface gaps effectively. While the PCM absorbs heat, it completely wets-out across the surface achieving an extremely thin bond line, providing excellent temperature control, close contact between surfaces, and minimal thermal resistance. Once the phase change temperature is first exceeded, optimal thermal performance is maintained above and below the melt temperature. Phase Change Materials are best for thermally conductive applications that require good wet out on surfaces with little or no force. While the PCM is soft or in its liquid state, excessive pressure will squeeze out extra material from in between the surfaces.
- Adhesives: provide both thermal conductivity and strong adhesion, they can be used where no mounting holes are available. Thermal adhesives create a strong mechanical bond between surfaces while offering high heat transfer and high voltage isolation. These specialized resins are mixed with thermally conductive fillers like ceramics or metallic particles that enable heat to easily transfer through the material and can act as both a TIM and a mounting method to reduce the amount of mounting hardware utilized in a product or application. Typically, adhesive compounds offer low shrinkage and coefficients of thermal expansion comparable to copper or aluminium and depending on the chemistry they easily bond to metals, ceramics, most plastics and a wide variety of other materials.
- Advanced Carbon-Based TIMs: utilize materials like Graphite, Carbon Nanotubes (CNTs) and graphene for their high thermal conductivity. With low mass and high heat transfer capabilities, Carbon-Based TIMs are high performance, high heat spreading thermal interface materials available in ultra-thin configurations which makes them an ideal solution for lightweight applications.
- Solder and metallic TIMs: solders are increasingly being explored as thermal interface materials because of their exceptional thermal conductivity. However, they can also introduce stresses stemming from coefficient of thermal expansion (CTE) mismatches. Despite their outstanding inherent performance, comprehensive microscopic modelling of solder TIMs' thermal performance is scarcely found in literature. This is mostly due to the traditionally satisfactory performance of solders, coupled with the preference for polymer TIMs, which are more cost-effective and easier to implement compared to their solder counterparts.

5.4.2 Key Parameters for TIMs Selection and Optimization

As discussed in the introduction, the TIM acts to connect the different parts of a thermal solution. After inserting a TIM between the solid surfaces, the effective thermal resistance, R_{th}, at the interface will have two components, i.e., the bulk resistance, R_{bulk}, of the TIM arising from its finite thermal conductivity and the contact resistance, R_c between the TIM and the adjoining solids. R_{th} may be expressed as:

$$R_{th} = \frac{BLT}{k_{TIM}} + R_{C1} + R_{C2}$$

where BLT is the bond-line thickness of the TIM, k_{TIM} is the thermal conductivity of the TIM, and R_{c1} and R_{c2} are the contact resistances of the TIM with the two adjoining surfaces. One of the goals of thermal design is to reduce R_{th}. This can be accomplished by reducing the BLT, increasing the thermal conductivity and reducing the contact resistances R_{c1} and R_{c2}.

BLT reduction can be accomplished by decreasing the TIM thickness. BLT is a function of parameters such as application pressure in bringing the two contact surfaces together and particle volume fraction. Since the yield stress of the TIM increases with increasing filler loading, BLT is higher for higher volume fraction. Therefore, there are two competing effects with regard to filler loading for the thermal resistance of the TIM: k_{TIM} increases and BLT also increases with increasing filler volume fraction at the same pressure, which leads to an optimal filler loading for the minimization of R_{TIM}.

The thermal conductivity of a TIM is typically enhanced by loading a soft, sometimes liquid-like polymeric material matrix with conducting solid particles, such as aluminium, alumina and boron nitride. The TIM's thermal conductivity depends on the filler material's thermal conductivity, volume fraction, and the interface's contact resistance. To increase the k_{TIM} it is possible to act on the filler type or by increasing the filler content, even though high-volume fraction can result in high interface resistance between the filler and the particles due to difficulty to wet the surfaces of the particles with the polymer matrix.

Contact resistances of TIMs are function of the surface roughness of the substrates, the nominal area of heat transfer, and the real area of heat transfer. The real area of heat transfer is smaller than the nominal area because of the trapped air in the valleys of a microscopically rough surface of the substrates. Based on this, a few general design guidelines to minimize contact resistance comprise increase pressure, decrease surface roughness, increase thermal conductivity of the TIM, and increase capillary force by changing the surface chemistry, that means by improving the rheology of TIM.

Other parameters to be considered are thermal conductivity and rheology. Timely choices of fillers impact thermal conductivity. Common materials include graphite for conductive needs, and boron nitride for non-conductive applications. Table 5-7 reports main filler types used in TIMs as well as their advantages and drawbacks, to be considered in TIM design phase and/or selection. Adjusting filler content is also crucial to enhance thermal conductivity but can increase costs significantly.

Rheological properties dictate how TIMs engage with surfaces. Liquid types offer excellent reduction in interfacial resistance but may require curing and are prone to pump-out. Solid and adhesive TIMs provide reliable adhesion and gap control while maintaining ease of handling.

Effective thermal management through TIMs is foundational for the performance and longevity of mobility electronics. Advances in TIM composition, filling, and application methods highlight ongoing improvements and address the growing complexities of automotive thermal management systems.

Table 5-7: Main filler types used as TIMs.

Filler Type		Benefits	Issues
Electrically conductive	Graphite	High TC, cheaper than BN	Dispersion in polymer matrix (filler combination needed)
	Graphene	Very high TC	Not mature for industry (exfoliation costs)
Electrical insulating	Boron Nitride (BN)	High TC	Expensive (processing cost)
	Alumina (Al_2O_3)	Medium TC, cheap	Abrasive for mixing equipment
	Aluminium oxide ($Al(OH)_3$)	Cheapest, flame retardant	Low TC, need high amount

5.4.3 Considerations

This section briefly described the role of TIMs in overcoming heat dissipation challenges, summarizing the scientific and theoretical frameworks underlying such materials and emphasizing the need to minimize thermal resistance to enhance heat conduction at interfaces when compared to thermal conductivity. The importance of reducing the thermal resistance through various strategies and of minimizing contact thermal resistance by enhancing effective interface contact and improving bonding strength has been outlined; numerous studies that have contributed valuable insights into these areas are available in literature.

Looking to the future, the field of TIMs is poised for continued innovation. Future research will focus on integrating novel materials, exploring advanced manufacturing techniques, and deepening the understanding of thermal transport mechanisms at the nanoscale.

6. Abbreviations

Term	Definition
2DEG	Two-Dimensional Electron Gas
AC	Alternating Current
AMB	Active Metal Brazed
AMC	Active Miller-Clamp
DBC	Direct Bonded Copper
DC	Direct Current
HEMT	High-Electromobility Transistor
HiPE	High Performance Power Electronics Integrations
IGBT	Insulated-Gate Bipolar Transistor
IMS	Insulated Metal Substrate
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
TIM	Thermal Interface Material
WBG	Wide Bandgap
HTCC	High-Temperature Co-Fired Ceramic
LTCC	Low-Temperature Co-Fired Ceramic

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